Small-Signal Modeling of a Single-Switch AC/DC Power-Factor-Correction Circuit
Guangyong Zhu, Huai Wei, Peter Kornetzky, and Issa Batarseh, Senior Member, IEEE

Abstract—In this paper, a small-signal model for a new single-switch single-stage switched-mode power-factor-correction (PFC) converter is presented. The model is obtained by applying the small-signal perturbation technique to the circuit equations derived from the state-space averaging method. By applying the perturbation and averaging techniques over one switching cycle, the dc and small-signal equivalent circuit representations of this converter are derived. The result shows that this converter exhibits the transfer characteristics of a second-order low-pass system for the output-to-input transfer function and that of a combined second-order low-pass and band-pass system for the output-to-control transfer function. The validity of the proposed mathematical model was verified by the given experimental results for a specified design example.

Index Terms—AC–DC converters, power factor correction, small-signal modeling.

I. INTRODUCTION

DURING the past two decades, power electronics research has focused on the development of new families of hard- and soft-switching converter topologies used in the design of dc–dc and ac–dc converters with active power factor corrections (PFCs). The goal is to design high-efficiency and high-power density converters with improved power factor and low electromagnetic interference (EMI). In recent years, as the new standards such as IEC 1000-3-2 became compulsory regarding limiting the total harmonic distortion (THD) and input power factor in power electronic circuits, researchers are actively seeking ways to shape the line current waveform to achieve THD and power factor that comply with international standards. Active PFC circuits that use pulsewidth modulation (PWM) switch-mode topologies such as the boost, buck–boost, and their derived ones have been used dominantly [8]–[11].

The steady-state analyses for a large number of such topologies are well documented, and their various dc control characteristics are well known. In addition to the steady-state behavior, the dynamic behavior is equally important and critical when it comes to the design of a robust control system for such converters. Control theory is applied to improve the performance of power electronics circuits such as the transient response, control accuracy, regulation capability and to reduce the effects of parameter variations as well as other disturbances. Over the last two decades, several control schemes have been reported in the literature, presenting various modeling techniques for the power stage [1]–[7].

A novel one-switch one-stage converter was proposed in [8], which features universal line voltage operation, near unity power factor, high efficiency, and low THD in the input current. Detailed steady-state analysis and design procedure of the converter was given in [8], whereas no dynamic analysis was reported. In Section II, a brief description of the circuit operation modes of the converter in each switching period is given. The state-space description for each operation mode can then be obtained and the averaged state matrices will be shown in Section III. Section IV presents the equivalent small-signal circuit model obtained from the relationships among the averaged state variables from which input-to-output and control-to-output transfer functions and their frequency responses are obtained. Based on these transfer functions, a discussion on the feedback controller design is also given to reveal the impact caused by the peculiar operation of the proposed converter. Simulation and experiment results are shown in Section V to verify the derived model. The conclusion is presented in Section VI.

II. REVIEW OF THE CIRCUIT OPERATION

The basic circuit diagram presented in [8] is redrawn in Fig. 1. Its key waveforms in a switching cycle are shown in Fig. 2. The circuit contains two stages: a boost converter in the input stage and a forward converter in the output stage. Both stages share the same switch. The output stage also contains a switched-capacitor network composed of two storage capacitors and a diode $D_2$ which operates in a series-charging, parallel discharging fashion. It is this switched-capacitor network that brings a number of favorable features
to the converter: low THD content in the input current, high power factor, simple circuit structure, and high efficiency.

Forward converters usually require additional demagnetizing schemes to prevent the transformer core from saturation. This requirement is automatically satisfied when the two storage capacitors are charged in series. Also, use of boost converters as PFC circuits, when operating in discontinuous conduction mode (DCM), introduces certain current distortion in the input current due to the slow discharging in the inductor current. This impact is significantly alleviated in the proposed converter when the sum of the two storage capacitor voltages is utilized to discharge the inductor current.

The converter has four operation modes within a switching cycle. Mode 1 begins when the power switch is turned on at $t = 0$. During this period, energy is transferred from the power source to the choke inductor and the inductor current increases linearly. At the same time, energy stored in the two storage capacitors $C_{s1}$ and $C_{s2}$ during the previous switching cycle is transferred to the load through two symmetrical branches in the secondary side of the forward transformer. As a result, current in the two leakage inductors $i_{pl}(t)$ and $i_{q2}(t)$ also increases until $t = t_1 = dT_s$ when the power switch is turned off. Here, $d$ is the duty cycle which is determined by the feedback loop, and $T_s$ is the switching period. During this period, we have the following current relations:

$$i_L(t) = \frac{V_i}{L} t$$
$$i_{pl}(t) = i_{q2}(t) = \frac{nV_{cs}}{nL_{p1}} t$$
$$i_{D3}(t) = \frac{2}{n} i_{pl}(t)$$

where $V_i$ is the average input voltage of the circuit in a switching period and $V_{cs}$ is the average voltage across the storage capacitor $C_{s1}$. $C_{s2}$ or $V_{cs1} = V_{cs2} = V_{cs}$.

In mode 2, diode $D_2$ conducts and $C_{s1}$ (or $C_{s2}$) is charged by $i_L(t)$ and $i_{q2}(t)$ (or $i_{pl}(t)$). The primary currents of the transformer, $i_{pl}(t)$ and $i_{q2}(t)$, decrease quickly due to the fact that the voltage across each of the leakage inductor is now the sum of the reflected output voltage and the storage capacitor voltage. Mode 2 ends at $t = t_2$ when $i_{pl}(t)$ and $i_{q2}(t)$ reach zero (they will not become negative due to the presence of $D_3$ on the secondary side of the transformer). In mode 2, we have

$$i_L(t) = \frac{V_i}{L} dT_s - \frac{2V_{cs} - V_i(t - dI_s)}{nL_{p1}}$$
$$i_{pl}(t) = i_{q2}(t) = \frac{nV_{cs} - V_0}{nL_{p1}} dT_s - \frac{nV_{cs} + V_0}{nL_{p1}} (t - dI_s)$$

and

$$i_{pl}(d + d_2)T_s = i_{q2}(d + d_2)T_s = 0$$

in which

$$d_1 = \frac{t_2 - t_1}{T_s} = \frac{nV_{cs} - V_0}{nV_{cs} + V_0} D$$

Mode 3 is an extended period of mode 2 in that the storage capacitors $C_{s1}$ and $C_{s2}$ are continuously being charged by current $i_L(t)$. During this period, the magnetic energy accumulated in the choke inductor $L$ and energy from the power source are continuously transferred to $C_{s1}$ and $C_{s2}$ in the same manner as that in mode 2. Therefore, the expression for $i_L(t)$ is also the same as that in mode 2. This mode ends when $i_L(t)$ decreases to zero at $t = t_3(t_3 - t_2 = d_2T_s)$ and

$$d_2 = \frac{t_3 - t_2}{T_s} = \frac{V_i}{g - 2V_{cs}} d - d_1$$

Mode 4 is known as the freewheeling stage and is used for regulation purposes only. Because of diode $D_3$, there is no energy transfer from the transformer to the load and the output voltage is maintained solely by the output capacitor $C_f$. The maximum regulation is achieved when the time duration of this stage reduces to zero. At $t = T_s$, this mode ends and a new switching cycle begins.

III. AVERAGED STATE-SPACE DESCRIPTION

In the modeling of nonresonant PWM converters, there are two most widely used approaches. The first one is the well-known state-space averaging method [2] that provides a generalized approach for a large class of PWM dc–dc converter. It is very straightforward and is based on the algebraic manipulation of a set of state-space equations of the converter circuit that are, for classical dc–dc converters, easily to be derived.

Another approach is the three-terminal switch model, known as the PWM switch model [5]. It is based on the observation that in a PWM converter, the switching action of the single-pole double-throw switch can be realized by an active switch (usually a controlled transistor) and a passive switch (usually a diode), and it is the only nonlinear component in the converter. Once its invariant property is determined, the average
equivalent circuit model of the converter can be derived and analyzed using the straightforward circuit analysis technique.

The PWM switch model is a powerful and convenient tool in the study of small-signal, transient response and controller design of PWM dc–dc converters [5], [7], [12]–[14]. Its application usually requires that the active and passive switches are to be appearing in pairs and to form a three-terminal network. There are, however, many converter circuits that are not presented in such direct forms and a two-port network in a generalized averaging model should be considered [14]. In this case, the port voltage and current relationship between the two ports often comes in nonlinear and more complex forms. Even for PWM dc–dc converters, there are cases that the active and passive switches are not tied together and are called separated PWM switches as was discussed in [12], where the equivalent linear circuit model for the switches was derived by the state-space equations. But the results can only apply to the continuous conduction mode (CCM) operation.

The dynamic modeling of PFC converters is a challenging one due to the fact that the conversion ratio widely changes within each half-line period and the steady-state operation point fluctuates at double the line frequency. However, it was shown theoretically and experimentally [7], [15] that the steady state can also be approximated as a linear system which fluctuates around a dc point determined by the rms value of the input voltage. Therefore, the small-signal analysis can be performed similar to that of a dc–dc converter with the input voltage replaced by the rms value of the rectified line voltage. Although most PFC converters can be analyzed with the PWM switch model or the two-port network, for the circuit described in Section II with separated switches, there exist complex relations among the port variables and these relations also rely on the derivation of the state equations. It is, therefore, easier to follow the state-space averaging approach in the derivation of the small-signal model of the converter.

To simplify the dynamic analysis, in the following discussion we neglect all the parasitics and assume \( C_{s1} = C_{s2} = C_s \) and \( L_{p1} = L_{p2} = L_p \) so that \( \dot{v}_{c1} = \dot{v}_{c2} = \dot{v}_{cs} \) and \( \dot{i}_{p1} = \dot{i}_{p2} = \dot{i}_p \). Also note that within one switching period, the rectified input line voltage can be considered to be constant and is denoted as \( V_g \).

Based on the converter operation modes described in Section II, the state-space equation for the state vector \( \mathbf{x} \) can be derived for each of the four operation mode over one switching cycle and are given by \( \mathbf{A}_i, \mathbf{B}_i, \) and \( \mathbf{C}_i \) for \( i = 1, 2, 3, 4 \).

Follow the averaging procedure, the averaged state-space equation, \( \mathbf{x} = \mathbf{A} \mathbf{x} + \mathbf{B} \dot{\mathbf{v}}_g, \mathbf{v}_0 = \mathbf{C} \mathbf{x} \), can be obtained over a switching period. The state matrices \( \mathbf{A}, \mathbf{B}, \) and \( \mathbf{C} \) are determined by

\[
\mathbf{A} = \mathbf{A}_1 d + \mathbf{A}_2 d_1 + \mathbf{A}_3 d_2 + \mathbf{A}_4 (1 - d - d_1 - d_2) \\
\mathbf{B} = \mathbf{B}_1 d + \mathbf{B}_2 d_1 + \mathbf{B}_3 d_2 + \mathbf{B}_4 (1 - d - d_1 - d_2) \\
\mathbf{C} = \mathbf{C}_1 d + \mathbf{C}_2 d_1 + \mathbf{C}_3 d_2 + \mathbf{C}_4 (1 - d - d_1 - d_2)
\]

and the results are given in (1). Since the converter operates in DCM, its steady-state and dynamic models can be obtained by using these matrices together with the expressions for the average inductor current given in (2)

\[
\mathbf{A} = \begin{bmatrix}
0 & 0 & \frac{d_1 + d_2}{C_s} & \frac{d_1 - d}{C_s} \\
0 & -\frac{1}{C_f R} & 0 & 2(d + d_1) \\
-\frac{2(d_1 + d_2)}{L} & 0 & 0 & 0 \\
-\frac{d - d_1}{L_p} & -\frac{d + d_1}{nL_p} & 0 & 0
\end{bmatrix}
\]

\[
\mathbf{B} = \begin{bmatrix}
0 \\
0 \\
\frac{d + d_1 + d_2}{L} \\
\frac{L}{0}
\end{bmatrix}
\]

\[
\mathbf{C} = \begin{bmatrix}
0 \\
1 \\
0
\end{bmatrix}
\]

\[
\dot{i}_L = \frac{v_g}{2L} d T_s, \quad \dot{i}_p = \frac{m_{cs} - v_0}{2nL_p} d T_s.
\]

In the next section, small-signal models are obtained from the above matrices by injecting perturbations.

IV. SMALL-SIGNAL MODEL

1) Mathematical Model: The steady-state model is derived by setting \( \mathbf{AX} + \mathbf{BV}_g = \mathbf{0} \) as is described by the following set of equations:

\[
\begin{align*}
(D_1 + D_2)I_L &= (D - D_1)I_p \\
nV_0 &= 2R(D + D_1)I_p \\
2(D_1 + D_2)V_{cs} &= (D + D_1 + D_2)V_g \\
n(D - D_1)V_{cs} &= (D + D_1)V_0 \\
I_L &= V_s DT_s / 2L \\
I_p &= (nV_{cs} - V_0) DT_s / 2nL_p.
\end{align*}
\]

The above equations determine the nominal steady-state operation point of the converter. Use of these equations in the converter design procedure was given in [8].

Small-signal relationship among state variables is derived by applying small-signal perturbations \( \dot{v}_g \) to the nominal input voltage \( V_g \) and \( d \) to the nominal duty cycle \( D \) as shown by

\[
v_g = V_g + \dot{v}_g, \quad d = D + \dot{d}.
\]

These perturbations result in variations in the state variables and the output voltage, i.e.,

\[
\mathbf{x} = \mathbf{X} + \mathbf{\dot{x}}, \quad v_0 = V_0 + \dot{v}_0.
\]

After linearizing the state equations, the general form of the small-signal transfer functions for the output-to-input \( H_s(s) \) and output-to-control \( H_d(s) \) can be obtained as

\[
H_s(s) = \frac{\dot{v}_g(s)}{\dot{v}_0(s)} = \frac{a_{21} b_{11}}{s^2 - (a_{11} + a_{22}) s + a_{11} a_{22} - a_{12} a_{21}}
\]

\[
H_d(s) = \frac{\dot{i}_p(s)}{\dot{d}(s)} = \frac{b_{22} (s - a_{11})}{s^2 - (a_{11} + a_{22}) s + a_{11} a_{22} - a_{12} a_{21}}
\]
where

\[
a_{11} = \frac{1}{C_s} \left[ \frac{2(D_1 + D_2)I_L}{V_g - 2V_{cs}} \right] + \frac{n(D - D_1)I_P}{nV_{cs} + V_0} - \frac{n(D - D_1)I_P}{nV_{cs} - V_0}
\]

\[
a_{12} = \frac{I_P}{C_s} \left[ \frac{D + D_1}{nV_{cs} + V_0} + \frac{D_1 - D}{nV_{cs} - V_0} \right]
\]

\[
a_{21} = \frac{2I_P}{C_f} \left[ \frac{D - D_1}{nV_{cs} + V_0} + \frac{D_1 + D}{nV_{cs} - V_0} \right]
\]

\[
a_{22} = \left[ \frac{1}{C_fR} + \frac{2(D + D_1)I_P}{nC_f} \right]
\]

\[
b_{11} = \frac{I_L}{C_s} \left[ \frac{D_1 + D_2}{V_g} - \frac{D + D_1 + D_2}{V_g - 2V_{cs}} \right]
\]

\[
b_{22} = \frac{2I_P}{nC_f} \left[ \frac{1}{D} + \frac{2nV_{cs}}{nV_{cs} + V_0} \right].
\]

For the converter with 50-W dc output power and the following set of circuit parameters: \( n = 0.27 \), \( L = 482.3 \mu H \), \( L_p = 80.9 \mu H \), \( C_s = 820 \mu F \), \( C_f = 900 \mu F \), and \( f_s = 50 \) kHz with input voltage 120 V(rms) and output voltage 50 V, the above expressions result in two transfer functions given as

\[
H_s(s) = \frac{394.7}{s^2 + 497.7s + 947.2}
\]

\[
H_d(s) = \frac{6531(s + 17.78)}{s^2 + 497.7s + 947.2}
\]

Frequency responses of these two transfer functions are shown in Fig. 3(a) and (b), respectively. It can be noticed that the system is highly damped, which is expected as the converter is operating in DCM condition. The two poles are well separated and are located around 0.5 and 80 Hz, respectively. These values can also be estimated by considering that the boost and forward converters are operating separately in DCM conditions using the above parameters. In this case, the steady-state storage capacitor voltage \( V_{cs} \) should be considered as the input of the forward converter and the sum of the two storage capacitor voltages (2 \( V_{cs} \)) be the output voltage of the boost converter. From (3) it turns out that \( V_{cs} \) is 194.4 V and the locations of the poles are about 0.31 Hz for the boost and about 78.3 Hz for the forward converter. They are very close to the values in Fig. 3. However, the converter system discussed in this paper is not just a mere cascaded connection of a boost converter with a forward one. It is rather a result of more tightly interconnected subsystems owing to the unusual operation of the switched-capacitor network as was mentioned in Section II. This impact is manifested by the presence of an additional left-half-plane (LHP) zero in the output-to-control transfer function which does not belong to either of the subsystem and should be considered in the design of the feedback controller.

In the closed-loop design of the PFC converter system, the controller should be designed properly such that the bandwidth of the voltage loop is significantly lower than the 120-Hz ripple frequency in the output to prevent degradation of the converter power factor. The crossover frequency of the loop gain is usually chosen around 10 Hz. For a DCM operating boost converter used as a PFC preregulator, a single type-II compensator in most cases can provide a reasonable phase margin (45°–60°) and a suitable gain attenuation (30–40 dB).

The introduction of another LHP zero normally increases the system stability. However, for the proposed converter, this zero is located at 2.8 Hz which provides significant phase leading at the desired crossover frequency (refer to Fig. 3), making it harder for a type-II compensator to achieve a suitable phase margin. Therefore, an extra phase-lagging network without phase inversion has to be added into the feedback loop to null the low-frequency zero. When implemented with an opamp, this network generates extra noise into the voltage loop and increases the number of components.

2) Equivalent Circuit Model: Fig. 4 shows the small-signal equivalent circuit, in which \( j_1, j_2, j_3, j_4, j_5, j_6, j_7, j_8, j_9, j_{10} \), and \( j_{11} \) are expressed in terms of the converter nominal operation values \( D, V_g, V_0, V_{cs} \), and circuit parameters such
as $n$, $L$, $L_p$, and $R$. These parameters are given as follows:

\[
   g_1 = \frac{2(D+D_1+D_2) V_{cs}}{2V_g - V_{cs}} I_L
\]

\[
   g_2 = \frac{2(D_1+D_2) I_L + n(D-D_1)}{nV_{cs}-V_0} - \frac{n(D-D_1)}{nV_{cs}+V_0} I_p
\]

\[
   g_3 = \frac{2(D+D_1)}{n} \left( \frac{1}{nV_{cs}-V_0} + \frac{1}{nV_{cs}+V_0} \right) I_p
\]

and

\[
   j_{11} = \frac{4V_{cs} I_L}{2V_{cs} - V_g}
\]

\[
   j_{12} = \frac{2(D_1+D_2)}{2V_g - V_{cs}} I_L
\]

\[
   j_{21} = \left( \frac{D_1+D_2}{V_g} + \frac{D+D_1+D_2}{2V_{cs} - V_g} \right) I_L
\]

\[
   j_{23} = \left( \frac{D-D_1}{nV_{cs}-V_0} - \frac{D+D_1}{nV_{cs}+V_0} \right) I_p
\]

\[
   j_{32} = 2 \left( \frac{D+D_1}{nV_{cs}-V_0} + \frac{D-D_1}{nV_{cs}+V_0} \right) I_p
\]

\[
   j_{33} = \frac{8V_{cs}}{nV_{cs}+V_0} I_p
\]

3) Simulation Results: According to the derived model of the converter circuit, Pspice simulation was also carried out and the results of the small-signal output-to-input and output-to-control frequency responses are depicted in Fig. 5(a) and (b), respectively. It is found from Figs. 3 and 5 that the theoretical transfer characteristics agree very well with the simulation results.

V. EXPERIMENTAL RESULTS

A prototype unit was constructed with the parameters given in Section IV in order to verify the small-signal model. Two types of measurements were performed: 1) input voltage is a rectified 60-Hz line voltage and 2) input voltage is a dc voltage with its value equals the rms value of the rectified line voltage. The results are given in Fig. 6(a) and (b).

It is shown from Fig. 6(a) and (b) that the measurement results under $V_g = 120 \ V_{ac}$ (rms) and $V_g = 120 \ V_{dc}$, respectively, agree very well with the two types of input voltages. The differences are only within 1 dB between the gains and within 6° between the phases; thus verifying the assertion that a PFC converter can be treated as a dc/dc converter with its input voltage equals the rms value of the rectified ac line voltage. This treatment greatly simplifies the analytical process and allows most of the well-understood dc/dc converter techniques to apply directly to the PFC applications.

Compared with the theoretical results shown in Fig. 3(b), however, it is found that they match each other only in the low-frequency range. There are significant differences when the frequency is higher than 300 Hz where the measured phase begins to increase and the slope of the measured gain begins to slow down. This phenomenon clearly indicates that there is still a zero in the high-frequency range that was not taken into account in our small-signal model. In practice, this zero is introduced by the nonideality of the output capacitor. To explain this point, its ESR (0.05 Ω) is considered in the model.
and the simulation result is given in Fig. 6(c). It is noticed that with this small ESR included, results from the measurement and the simulation are in good agreement.

Measurement of the frequency responses were also performed for different line conditions, and were compared to the simulation results according to the derived small-signal model. The experimental and simulated results are shown in Fig. 7(a) and (b) for $V_g = 110\,\text{V}_{\text{ac}}$, respectively. Fig. 8(a) and (b) shows the experimental and simulated results for $V_g = 150\,\text{V}_{\text{ac}}$, respectively. Under different input conditions, the difference between the measured and simulated results is within 2 dB in the magnitude. Discrepancy in the phase is within 5° for most of the measured frequency points except in the high-frequency range where this value is larger but is still limited within 10°. The reported results indicate that the proposed model
is accurate and is a good representation of the small-signal behavior of the converter.

VI. CONCLUSIONS

In this paper, a small-signal model for a single-switch single-stage PFC converter was developed using the state-space averaging technique. The underlined assumption in the derivation was that the steady-state condition can be determined by a dc input whose voltage equals the rms value of the rectified line input voltage. The assumption was verified experimentally, thus allowing the analytical method developed for the dc–dc converters to be applicable directly to the PFC circuit design.

A special property in the output-to-control transfer function was observed. This property is characterized by the presence of a low-frequency LHP zero which does not occur in either of the boost or forward converter when operating in DCM conditions. It is a result of the unique manner of the energy being transferred from the boost converter to the forward converter. The impact of this zero on the controller design was also discussed.

Finally, the effect of the ESR of the output capacitor on the dynamic behavior of the PFC circuit was illustrated. The developed mathematical and circuit models were verified by simulation and by the measurement data under different input line conditions. All the results are indicating the validity of the proposed models.

REFERENCES