Steady State Analysis of Zero-Voltage-Transition-PWM Converter with Power Factor Correction

Khalid Rustom, Jaber Abu Qahonuq and Issa Batarseh
School of Electrical Engineering and Computer Science
University of Central Florida
Orlando, FL 32816

Tel. (407) 823-0185 Fax (407) 823-5853

Email: batarseh@mail.ucf.edu

Abstract - A single-stage, ZVT-PWM, power factor correction converter is proposed in this paper. Zero-voltage switching for the main switch and zero-current switching for the auxiliary switch are realized by utilizing the leakage inductance of the output transformer and the capacitance of the switches. As a result, no additional resonant components need to be added. High frequency operation of the proposed converter makes the ac-dc power supply possible to be minimized in size and weight and the soft switching scheme will reduce the electromagnetic interference (EMI). The simplified driving circuitry again improves the overall efficiency and power density. Practically, the direct driving schemes of both the main and the auxiliary switches allows the proposed converter to operate in even high switching frequency and have good regulation capability. A 50-W 500-kHz prototype has been built in the laboratory to experimentally verify the analysis and simulation results.

I. INTRODUCTION

The growing concern about the harmonic pollution and with the new standards that introduced, there is a real demand on a clean power supplies with a low harmonics contents of the ac line currents. Yet the use of power supplies continues to increase and more distorted mains current is drawn from the line, resulting in lower power factor and high total harmonic distortion. This distortion problem becomes more serious when the loads become highly non-linear. Power Factor Correction (PFC) is becoming more and more common in single-phase off-line switching-mode power supplies, not only because low power factor limits the maximum available power drawn from mains, but also agency regulation requires that the harmonic current of the line current of mains-connected equipment remains below certain limits. For many years a great deal of effort has been made to develop efficient and cost-effective power factor correction schemes. As a branch of active PFC techniques, the single-stage technique receives particular attention because of its low cost implementation [1,2,3].

Moreover, with the residential and defense industries continuously demanding for even higher power density, switching mode power supply operating at high-frequency is required because at high switching frequency, the size and weight of circuit components can be remarkably reduced. But with the increasing of switch frequency, the switching loss becomes intolerable, resulting in very low conversion efficiency. Furthermore, the presence of leakage inductance in the high-frequency transformer and junction capacitance in the semiconductor devices causes the power devices to turn-OFF and turn-ON with more energy loss and noise. Because of this reason, the switching frequency of the traditional SMPS (Single Mode Power Supplies) is limited to 100kHz. To boost the switching frequency various soft-switching technique have been introduced to alleviate the switching losses [4,5].

In this paper, a single-stage soft switching power factor correction circuit is proposed. The principle of operation and the soft switching condition are presented along with simulation and some experimental results for a 50W @ 50kHz prototype.

II. PROPOSED CONVERTER AND ITS OPERATION

The proposed soft-switching converter in Fig. 1 is based on the hard-switching single-stage PFC converter with two bulk capacitor proposed first in [3]. Besides achieving zero-voltage transition (ZVT) for the main switch, the circuit also using an extra winding on the transformer core as a snubber,  to lower the voltage and the current stresses of the auxiliary switch. The diode  is added to prevent circulating current through  and  present the parasitic capacitance of  and  respectively.  and  are the leakage inductance of the primary side transformer  and  respectively.

The main waveforms and the equivalent circuits for the modes of operation are shown in Figs. 2 and 3, respectively.
Mode 1: $t_0 < t < t_1$

Initially, it is assumed that $S$ was $OFF$ and $C_s$ has an initial voltage of $V_{Cso}$ that is greater than $V_{in,rms}$. In this paper the input voltage will be assumed to be constant and equal to the $rms$ value of the line voltage $V_{in,rms}$. At $t = t_0$, the auxiliary switch $S_a$ is turned $ON$. $C_s$ and $L_m$, $L_{k1}$ form a resonant tank as shown in Fig. 3(a) along with $L_{k1}, L_{k2}$. The resonant in the auxiliary branch will be the dominant on the soft switching condition; other branches will have a small reflected effect due to the transformer turns ratio. The voltage across the capacitor $C_s$ will drop to $V_{in,rms}$ at ($t = t_1$). The key equations for this mode can be expressed as follows:

$$v_C(t) = \left[\frac{2\Delta V_o}{n_L} + V_{Cso}\right]\left[\frac{L_{bk}}{2\Lambda_{/n+1}}\right]\left[1 - \cos\omega(t-t_o)\right] + V_{Csp}\cos\omega t$$

$$i_{Li}(t) = \left[\frac{2\Delta V_o}{n_L} + V_{Cso}\right]\left[\frac{1}{n_L} - \frac{1}{2\Lambda_{/n+1}}\right]\left[\frac{L_{bk}}{2\Lambda_{/n+1}}\right]\left[\frac{1}{2\Lambda_{/n+1}}\right]\left[\frac{1}{\Lambda_{/n+1}}\right]$$

$$+ \frac{V_{Csp}\sin\omega t}{L_{bk}} - \frac{n_L}{L_{bk}} V_{o} t$$

$$i_{Li}(t) = 0 ; i_{Do}(t) = 0 \text{ (Very small)}$$

Where,

$$n = \frac{n_1}{n_2} ; n_o = \frac{n_r}{n_o} ; \omega_o = \frac{1/n_o + 1/\Lambda}{C_s L_{bk}}$$

Mode 2: $t_1 < t < t_2$

This mode starts when $v_C \leq V_{in,rms}$. The diode $D_i$ starts conducting a small current that will charge $L_i$. The effect of this mode on the resonant condition is very small and it has neglected effect on $I_{Li}$ too, so that the equations from mode 1 will be valid during this mode except for $i_{Li}$ that will be very small ($i_{Li}(t) \approx 0$). At the end of this mode ($t = t_2$), the capacitor voltage of the main switch $S$ reaches zero, allowing $S$ to be turned $ON$ at ZVS during any time after that. The switching interval for this mode is given by:

$$\Delta_2 = t_2 - t_o = \frac{1}{\omega_o} \cos^3\left[\frac{-V_{Csp}L_{bk}(2+n/n_o)}{2n_L V_o [L_{bk} + L_o (2+n/n_o)]} + 1\right]$$
Mode 3: \( t_3 < t < t_4 \)

This mode will start after \( v_{Cs} \) reaches zero \( D_S \) will conduct the capacitor current and \( L_i \) will start effectively charging through the input voltage. \( L_{ak} \) will start linearly discharging. This mode will last until the \( i_{Ds} \) reaches zero. We can turn \( ON \) the main switch \( S \) at any time during this mode preferably at the end of this mode. A second resonant condition will occur if \( S \) is kept \( OFF \) that will result in raising the voltage across \( C_s \) and ZVT will be lost. Equations for this mode will include:

\[
i_{Lak}(t) = \frac{-n_oV_o}{L_{ak}}(t-t_2) + i_{Lak}(t_2)
\]

\[
i_{Li}(t) = \frac{V_{in,rms}}{L_i}(t-t_2)
\]

\[
i_{Do}(t) = 0
\]

The time interval is given by,

\[
t_3 - t_2 = \frac{i_{Lak}(t_2)\left[1 - (n_o/n)\right]}{n_oV_o\left(1 - (n_o/n) + \frac{n}{n_oL_m}\right)} + \frac{V_{in,rms}}{L_i}
\]

where \( i_{Lak}(t_2) \) is the initial inductor current at \( t=t_2 \).

Mode 4: \( t_3 < t < t_4 \)

After turning \( S \) \( ON \) at \( t = t_3 \), the choke current continues to charge up linearly. This period ends when the leakage inductor current \( i_{Lak} \) reaches zero and \( D_L \) reverse biased. We can turn \( OFF \) the auxiliary switch \( S_a \) at any time after this mode With ZCS. The equations for \( i_{Lak}, i_{Li} \) and \( i_{Do} \) from mode 3 will be valid through out this mode.

\[
t_4 - t_3 = \frac{i_{Lak}(t_3)L_{ak}}{n_oV_o}
\]

Mode 5: \( t_4 < t < t_5 \)

After turning \( S_a \) \( OFF \) at \( t = t_4 \), the inductors \( L_{ak} \), \( L_{k2} \) will start charging through the stored energy capacitors \( C_{p1}, C_{p2} \) respectively. \( D_L \) will prevent the negative current in \( L_{ap} \) and output current will increase linearly. This mode ends when we turn the main switch, \( S \), \( OFF \).

\[
i_{tp1} = i_{tp2} = \frac{V_{cp} - nV_o}{L_K}(t-t_4)
\]

\[
i_{Do} = 2ni_{tp1}
\]

\[
i_{Li}(t) = \frac{V_{in,rms}}{L_i}(t-t_4) + i_{Li}(t_4)
\]

where \( i_{Li}(t_4) \) is the initial inductor current at \( t=t_4 \).

Where \( V_{cp} \) is the average stored voltage in the capacitors \( C_{p1} \) and \( C_{p2} \).

Mode 6: \( t_5 < t < t_6 \)

At \( t = t_5 \), \( S \) is turned \( OFF \). The main switch output capacitor \( C_s \) is quickly charged up by the current \( i_{Li} \) to the maximum value, \( 2V_{cp} \). Under the constraint of KCL, both the storage capacitors, \( C_{p1} \) and \( C_{p2} \) are being charged by the current \( i_{tp1} + i_{tp2} \) during this operation period. With the inductor current \( i_{Li} \) decreasing linearly, magnetic energy stored in the choke is being converted into electric energy and being stored into the storage capacitors. Thus the energy loss of the storage capacitors during the previous Mode is being recovered. Because \( i_{tp1} \) and \( i_{tp2} \) are relatively small, the duration of this mode can be neglected (\( \Delta t_6 = t_6 - t_5 \approx 0 \)).

\[
i_{tp1}(t_6) = i_{tp2}(t_6) = i_{Do}(t_6) = 0
\]

\[
v_{Cs}(t_6) = 2V_{cp}
\]

\[
i_{Li}(t_6) = \frac{V_{in,rms}}{L_i}(DT + t_3 - t_2)
\]

Mode 7: \( t_6 < t < t_7 \)

The choke inductor current, \( I_{Li} \), continues to decrease linearly. Owing to the existence of diode \( D_o \), the primaries of the transformer present very high impedance with the currents through the windings can be negligible. This period ends when the choke inductor current reaches zero.

\[
i_{Li}(t) = \frac{V_{in,rms} - 2V_{cp}}{L_i}(t-t_6) + i_{Li}(t_6)
\]

\[
t_7 - t_6 = \frac{i_{Li}(t_6)L_i}{V_{Cs} - V_{in,rms}}
\]

Mode 8: \( t_7 < t < t_0 + T \)

This is a freewheeling stage for regulation purpose. During this mode the voltage across the capacitor \( C_s \) reduced from \( 2V_{cp} \) to \( V_{cw} = V_{cp} \) because it inters a pre resonant stage.
III. SOFT-SWITCHING CONDITION

Soft-switching is maintained for this circuit if the main switch S turned ON during mode 3 as explained in the circuit operation where:

\[ t_2 \leq t \leq t_3 \]

IV. COMPUTER SIMULATION AND EXPERIMENT RESULTS

Using the component values shown in the schematic (Fig 4) produces the result shown in Fig 5, which verifies the theoretical analysis.
As can be noted, the simulated waveforms are the same as theoretical waveforms. Also, the ZVS and ZCS are achieved for the main switch and auxiliary switch, respectively.

A 50-W, 500-kHz prototype has been built in the laboratory to experimentally verify the analysis. The results agree well with the computer simulation. In Fig. 6, the lower waveform is the drive signal of the power MOSFET and the upper waveform is the voltage across the MOSFET. It’s shown that drive signal starts rising after the voltage across the MOSFET drops down to zero, which is zero voltage switching. However, from Fig. 6, we can see the oscillations that would lead to EMI problems. It’s expected to be reduced by using a transformer with a smaller parasitic capacitance and inductance.

VI. CONCLUSION

Due to high frequency operation, the proposed converter makes the design of unity power factor ac–dc power supply possible with improved size and weight. At the same time, the active single-stage PFC techniques help to reduce the component count and cost and by utilizing the leakage inductance of the output transformer and the capacitance of the switches, so that no additional resonant components are need to be added. Moreover, the proposed converter uses a grounded auxiliary switch so that the isolated driving circuit is not required. We believe that the proposed converter could be considered as a strong competitor in low power application.

REFERENCES