A SINGLE-STAGE POWER FACTOR CORRECTION CONVERTER
With SOFT-SWITCHING OPERATION

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Abstract: A single-stage power factor correction converter with soft-switching will be proposed in this paper. The converter topology is derived by adding a resonant circuit to an existing S^4 PFC converter. As a result, zero-voltage-switching and zero-current-switching are achieved for the main switch and the auxiliary switch, respectively. High frequency operation of the proposed converter makes the power supply possible to be minimized in size and weight.

I. INTRODUCTION

With the advanced development of power semiconductor devices, more and more switch-mode power supplies (SMPSs) and other power switching circuits are used in modern power system. Due to the non-linear behavior of power switched circuits, distorted currents are normally drawn from the line, resulting in low power factor (PF) (usually less than 0.67) and high total harmonic distortion (THD). Declining power quality in many power electronic systems has become an important issue.

Basically, two techniques have been commonly used in improving PF and reducing THD, i.e., continuous conduction mode (CCM) shaping technique and discontinuous conduction mode (DCM) voltage following technique. The former technique mainly deals with the control strategies applied to the power converters. A number of new control methods, such as charge control and nonlinear carrier control, have been proposed [1,2] to reduce the complexity of the control circuit and enhance system dynamic response. Yet the latter technique stresses on the effectiveness of the circuit topologies of the power converters, resulting in several efficient ac-dc converters in the open literature [3-5].

The DCM voltage following technique is well suitable for low power application because of its low-cost implementation. However, there exists another demand in certain applications, that is high power density, which may not be satisfied by a hard-switching DCM voltage follower. To make the switching power supply into smaller size, high frequency operation becomes necessary. Unfortunately, the power semiconductors in most of the DCM voltage followers switch at high current and high voltage (usually 400V to 600V), resulting in intolerable switching losses at high frequency operation. In order to relieve the switching losses, soft-switching technique is applied.

In this paper, a single-stage DCM power factor correction (PFC) circuit with zero-voltage-switching (ZVS) is proposed. The principle of operation of the proposed converter will be given in Section II. Its steady state analysis will be presented in Section III. Simulation results will be given in Section IV. Finally, in Section V, conclusions will be drawn.

II. PROPOSED ZVS CONVERTER AND ITS CIRCUIT OPERATION

In reference [3], a single-stage single-switch (S^4) PFC converter with two bulk capacitors was proposed (Fig. 1). This converter degrades the cost by using two storage capacitors to share the dc bus voltage. When the switch is turned on, the input inductor draws energy from the line, meanwhile, the storage capacitors C51 and C52 supply power through the transformer. When the switch is turned off, the input inductor current charges the storage capacitors. Near unity power factor can be obtained since the choke inductor operates in DCM.

![Fig. 1 Existing ac-dc S^4 converter](image)

However, high power density can not be achieved due to the fact that the power switch operates under hard-switching with higher than 400V drain-source voltage. In order to create a ZVS condition for the power switch, an auxiliary switch S_n, two resonant inductors, L_1 and L_2, a resonant capacitor C_n, and a diode D_n are introduced, shown in Fig. 2. To relieve the capacitive turn on loss on the auxiliary switch, low output capacitance MOSFET should be considered in selecting S_n.
Fig. 2 The proposed soft-switching PFC converter

In each switching cycle, with the auxiliary switch $S_a$ turning on, a short interval of resonant takes place during which the main switch turns on with ZVS. The cyclic operation of the proposed converter is almost the same as its hard-switching counterpart except that a resonant mode is inserted. The switching waveforms are shown in Fig. 3 and the switching periods are described as follows by assuming that capacitor voltages $V_{C1} = V_{C2} = V_C$, are constant and the line voltage is $V_L$ in one switching cycle.

Before the auxiliary switch is turned on, the main switch is open, and its output capacitor holds a voltage of $2V_C$. The resonant inductors carry zero current. Let's start the cyclic operation when the auxiliary switch is turned on at $t_0$.

Fig. 3 Theoretical waveforms of the proposed converter

Switching Period 1: At $t = t_0$, the auxiliary switch $S_a$ is turned on. A resonance takes place firstly among $C_{sw}$, $C_r$, $L_{r1}$ and $L_{r2}$. The thicker line in Fig. 4(a) shows the resonance loop during this switching period.

It can be shown that in order to create zero-voltage-switching condition for the main switch $S$, we must design the resonant capacitance $C_r$ to be larger than the output capacitance $C_{sw}$ of the main MOSFET switch, i.e., $C_r / C_{sw} > 1$.

Fig. 4 Equivalent topologies for the six switching periods
Switching Period 2: With the switch voltage \( V_{sw} \) decreasing to zero, diode \( D_{sw} \) conducts. The input inductor \( L \) is magnetizing in this period. The resonance continues among \( C_a, L_1 \) and \( L_2 \), as shown in Fig. 4(b).

In this period, the main switch is turned on with ZVS. This period ends when the resonant capacitor voltage reaches zero.

Switching Period 3: With the capacitor voltage \( V_C \) resonant to zero, diode \( D \) turns on. Since \( S_{-L_2-D_{-L_1-S}} \) forms a free-wheeling loop, as shown in Fig. 4(c), the resonant inductor keeps a constant current. The auxiliary switch can be turned off with zero-current-switching (ZCS) at anytime when the resonant inductor current \( i_L \) becomes negative. The transformer primary windings \( N_{p1} \) and \( N_{p2} \) transfer energy to its secondary \( N_t \) from energy storage capacitors \( C_{a1} \) and \( C_{a2} \), respectively. The input inductor continues magnetizing, absorbing energy from the line.

Switching Period 4: The main switch is turned off. The switch output capacitance \( C_{sw} \) is quickly charged to \( 2V_C \) by input inductor current \( i_L \) and resonant inductor current \( i_L \), as shown in Fig. 4(d), then diode \( D_1 \) starts conducting to clamp the main switch voltage. Assuming the switch voltage reaches \( 2V_C \) with zero time, the resonant inductor current is increasing linearly and the primary winding currents are decreasing linearly. This switching period ends when both the resonant inductor current and the primary winding current reach zero. Because \( L_1 \) and \( L_2 \) are very small, the duration of this period can be neglected in steady state analysis.

Switching Period 5: Input inductor continues to demagnetize until all the magnetic energy is released to charge the storage capacitors (Fig. 4(e)).

Switching Period 6: With the input inductor current decreasing to zero, diode \( D_2 \) turns off (Fig. 4(f)). All the voltages and currents remain constant. The converter is waiting for the next driving signal \( S_n \) to start a new switching cycle.

III. STEADY STATE ANALYSIS

A. Storage capacitor voltage

To improve the input power factor and stabilize the output voltage, two higher value storage capacitors are used in the proposed converter. In steady state operation, the storage capacitor voltages can be considered as constant. It can be shown that the higher the storage capacitor voltage, the higher the input power factor can be obtained. Unfortunately, almost all the components voltage stresses are directly related to the storage capacitor voltage. In practical design, some trade off must be made.

In order to look into the storage capacitor voltage, let’s define the following voltage ratio:

\[
M_i = V_{o}/V_C.
\]

It can be shown that the output to storage capacitor voltage ratio can be described as the following equation,

\[
\frac{n}{k_t} \frac{T_s}{T_s} \left( D - \Delta t_1 + \Delta t_2 \right)^2 \left( 3 - n \frac{M_i}{M_1} \right) \left( 1 - n \frac{M_i}{M_1} \right) \left( \frac{1 + \frac{M_i}{M_1}}{1 + \frac{M_i}{M_1}} \right) = 1,
\]

where,

\[
D \Delta t_1 (t_1 - t_0) / T_s; \quad k_t = L_t / L;
\]

\[
\Delta t_1 / T_s = 0.5 f_{a1} \left[ 1 - \left( \pi \sqrt{1 + k_c} \right) \cos^{-1} k_c \right];
\]

\[
\Delta t_2 / T_s = 0.5 f_{a2} \left( \sqrt{1 + k_c} - \pi \tan^{-1} \sqrt{k_c - 1} \right);
\]

\[
k_c = \frac{C_r}{C_{sw}}; \quad f_{a1} = 2 \pi \sqrt{2 L_r C_r f_s}.
\]

Figure 5 shows output to storage capacitor voltage ratio under different loads in term of duty ratio. It can be seen that when \( D > 0.2 \), we have

\[
M_i \approx 1/n.
\]

![Fig. 5 Output to storage capacitor voltage ratio](image)

B. Ac-dc conversion ratio

Since the input voltage of the ac-dc converter is 60Hz sinusoidal, we define the ratio of output voltage to rms value of line voltage as ac-dc conversion ratio, i.e.,

\[
M \Delta = \frac{V_o}{V_{rms}}.
\]

Considering power balance \( (V_{rms} I_{rms} = V_o^2/R) \) in steady state, the ac-dc conversion ratio is given by,
\[ M = \frac{1}{2\sqrt{2}} \left( M_1 + \sqrt{M_1^2 + \frac{4}{T_n} \left( D - \Delta T/T_1 \right)^2} \right) \] (5)

Figure 6 gives the conversion characteristic under deferent load time constants.

E. Practical challenge
Since there exists output capacitance in the auxiliary switch Sa, high peak parasitic ringing occurs during the switch is turned off, resulting in difficulty in selection of the auxiliary switch. To block the auxiliary switch voltage, the resonant tank is modified as shown in Fig. 7. Two resonant capacitors are used on each side of the auxiliary switch. Between each resonant capacitor and the switch, two diodes are connected to block the switch voltage at \(2V_{C1}\). The block diodes conduct only a short time in one switching cycle, so only low rating is required.

![Proposed converter with voltage clamp](image)

Fig. 7 Proposed converter with voltage clamp

IV. EXPERIMENTAL RESULTS

The proposed soft-switching PFC converter has been simulated on PSPICE with the following parameters:

- \( L = 20\mu\text{H} \)
- \( C_s = 200\mu\text{F} \)
- \( C_o = 2\mu\text{F} \)
- \( n = 4 \)
- \( R = 50\Omega \)
- \( C_{sw} = 510p\text{F} \)
- \( L_{r} = 3\mu\text{H} \)
- \( C_r = 3.5n\text{F} \)
- \( C_{sa} = 55p\text{F} \)

![Simulated line voltage](image)

Fig. 8 Simulated line voltage (upper) and input inductor current waveform over one line cycle (lower)

![Simulation waveforms](image)

Fig. 9 Simulation waveforms of the proposed PFC converter

Figure 8 shows the input inductor current over line cycle. Due to DCM operation of the input inductor, the peak current follows the line voltage, implying high power factor.

The simulated switching waveforms are shown in Fig. 9. As it can be seen, zero-voltage turning on for the main switch and zero-current turning off for the auxiliary switch have been achieved. The voltage across the auxiliary switch has been successfully clamped below 500V.

V. CONCLUSIONS

A single-stage power factor correction converter with soft-switching is proposed in this paper. By introducing resonant modes, zero-voltage-switching for the main switch and zero-current-switching for the auxiliary switch are obtained. As a result, high switching losses have been relieved so that the proposed single-stage power factor correction converter can operate in high frequency with smaller size magnetic components.

REFERENCES


V-225