LARGE-SIGNAL SIMULATION OF A DISTRIBUTED POWER SUPPLY SYSTEM WITH POWER FACTOR CORRECTION\(^1\)

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ABSTRACT-A large signal simulation for a distributed power supply system is presented in this paper. The system is composed of two parallel-connected switched-mode power factor correction (PFC) converters utilizing central limit control technique. This technique allows one voltage loop compensator to be shared by all the PFC converters. Design of such a compensator is discussed and the system performances with regard to unequal cable resistances and load changes are reported. The resulting system features a universal input with a power factor greater than 0.98 and provides excellent current sharing among the converter modules.

1. INTRODUCTION

In the past, research efforts in power electronics research have been mainly concentrated on individual converter design and seldom on its performances and interactions within the building block modules of a larger power supply system. Power supply engineers used to select a centralized power system that uses only a single power converter for the design of a complicated system. In a centralized power system, a bulky power converter processes all the power and provides the final voltages required by the loads. This arrangement may lead to a system with low reliability and unnecessary complexity. Recently, distributed power systems (DPSs) attracted much attention. The DPS structure distributes the needed power among several smaller power converters and then connects them in parallel to power one or several loads. This structure allows the smaller power supply systems to be manufactured into standard "plug-in" modules to enable the ease of system expansion and maintenance. It also promotes the system reliability by providing redundancy.

Another important issue in power electronics research is the power quality control. As new standards such as the IEC 1000-3-2 became compulsory regarding limiting the total harmonic distortion (THD) of power electronic equipment, researchers are actively seeking ways to shape the line current waveform to achieve low THD and high power factor. Active power factor correction (PFC) circuits that use PWM switch-mode have been used extensively and numerous topologies have been reported [1-2].

However, topics of DPS and PFC are usually discussed separately in the open literature. Stability and dynamic characteristics regarding parallel operation of dc-dc converters have been studied extensively with the loop gain concept and classical control theory [4,5]. Interactions between line conditioners and load converters were also specified [6,7], where design guidelines ensuring stable operation were developed in terms of output impedance and input impedance of line conditioners and load converters, respectively. In these studies, the parallel-connected converters were assumed identical so that a reduced-order power stage model can be used to avoid tedious calculations. In contrast, to the best of our knowledge, paralleling of PFC converters has not been thoroughly studied. Fig. 1 shows a typical DPS in communication systems in which a number of ac-dc PFC converters provide the necessary dc power. In a DPS with PFC converters, line harmonic current suppression is also a critical issue in addition to other considerations in paralleling dc-dc converters. In this paper, considerations in designing the control loop are discussed to achieve high power factor and equal load sharing between two parallel-connected converters. In the next section, a brief description of the PFC converter to be used will be given. The current sharing control technique and feedback loop design will be presented in Section 3. Since current sharing is considered, reduced-order power stage model can not be used and actual circuit simulation has to be conducted to show the results. System performances with regard to unequal cable resistances and large load changes will be shown in Section 4, with the conclusions given in Section 5.

Fig. 1. Block diagram of a typical distributed power system.

\(^1\)This project is funded by NASA-KSC under the STTR program contract number NAS10-98064, 10/22/1998
2. DESCRIPTION OF THE PFC CIRCUIT

In this DPS structure, we select a single-switch, single-stage PFC circuit from the recent literature [2]. Its topology and key waveforms are shown in Fig. 2(a) and (b), respectively. This circuit uses a boost converter as the input stage and a forward converter as the output stage. Detailed analysis of the circuit can be found in [2]. Its operation within a switching cycle is briefly summarized below:

The converter has four operation modes. Mode 1 begins when the power switch is turned on at \( t=0 \). During this period, energy is transferred from the source to the choke inductor \( L \). At the same time, energy stored in the two storage capacitors \( C_{s1}, C_{s2} \) is transferred to the load through two symmetrical branches in the primary side of the transformer. As a result, leakage inductor currents \( i_{Lp}(t) \) and \( i_{Lq}(t) \) also increase until \( t=t_2 \) when the power switch is turned off. In mode 2, diode \( D_2 \) conducts and \( C_{s1} \) (or \( C_{s2} \)) is charged by \( i_{Lp}(t) \) and \( i_{Lq}(t) \). Mode 2 ends at \( t=t_2 \). When \( i_{Lp}(t) \) and \( i_{Lq}(t) \) reach zero. Mode 3 is an extended period of mode 2 in that \( C_{s1} \) and \( C_{s2} \) are continuously being charged by current \( i_s(t) \). During this period, the magnetic energy accumulated in the choke inductor \( L \) and energy from the power source are continuously transferred to \( C_{s1} \) and \( C_{s2} \) in the same manner as that in mode 2. This mode ends when \( i_s(t) \) decreases to zero at \( t=t_3 \). Mode 4 is known as the freewheeling stage and is used for regulation purposes only. At \( t=t_4 \), this mode ends and a new switching cycle begins.

3. CLOSED-LOOP COMPENSATOR DESIGN

Uneven load current distribution among parallel-connected modules in DPS degrades system performance and reliability. One of the factors affecting uneven load sharing is the unbalanced cable resistances from the load to each module output. Among various approaches the central limit control (CLC) scheme [8] shown in Fig. 3 is an effective one to control the current delivered by each module. In CLC, a common reference voltage and one compensator are used. In order to achieve the desired current sharing, current error signal of each converter is added to the output of the error compensator and the result is used as the control voltage of each PWM modulator. CLC scheme effectively minimizes the influence of circuit parameter discrepancies of each module on its output current and features stable current sharing and precise output voltage regulation in dc/dc applications.

In many high power applications, PFC converters operating in continuous conduction mode (CCM) are usually implemented with the current mode control and a current loop is included. In these converters, the compensator and CLC outputs \( v_{i1} \) and \( v_{i2} \) are used to determine the magnitude of the sinusoidal reference current. Thus the scheme shown in Fig. 3 is suitable for PFC converters in both CCM and DCM modes. In this scheme, we included the cable resistance for converter \#1 (\( R_{i1} \)) and converter \#2 (\( R_{i2} \)) Current sharing is controlled by properly distributing error signals \( i_{i1}, i_{i2} \) to each converter.

![Fig. 3. Block diagram of a CLC scheme.](image)

The major concern in simulating such a system is in the design of compensator transfer function \( G_c(s) \) to avoid unstable operation when the source voltage and/or load are subject to large variations. These variations change the operation conditions of the converter circuits and therefore affect their dynamic characteristics. This effect becomes more pronounced when these converters are operating in DCM conditions. Fig. 4 shows the bode plot of the control to output voltage transfer function for each individual PFC converter given in Fig. 2 under different line and load conditions. These transfer functions were obtained from the model developed in [3].

Unlike in dc/dc power supplies, design of ac/dc converters requires that the crossover frequency of the voltage loop gain should be no greater than one-fourth or
one-third of the line frequency to avoid degradation of the input power factor. Unfortunately the PFC power stage experiences a noticeable variation in its frequency response during this frequency range for the four specified operation conditions, as is shown in Fig. 4. In addition, the power stage exhibits a relatively small phase delay in this frequency range (approximately 20°-40°), which makes it impossible to compensate with a common 2nd order compensator. A systematic approach led to a 3rd order compensator design with its transfer function given as:

\[ G_c(s) = \frac{39270(s + 52.5)}{s(s + 210)(s + 105)} \]

Fig. 4. Control-to-output voltage frequency response of the ac-dc converter.

With the above transfer function, voltage loop gain for each converter can be depicted when voltage sampling gain and modulator gain are considered and it is shown in Fig. 5. It is seen that this compensator results in a 45° phase margin at crossover frequency \( f_{c} \approx 16.7 \text{Hz} \) when the line is 220VAC. It also gives 45°-55° phase margins for other line and load conditions.

4. SIMULATION RESULTS

The DPS utilizing CLC as shown in Fig. 3 was simulated by Pspice using two 50VDC output voltage modules operating at 50kHz switching frequency. Stability and current sharing ability were examined under different line and load conditions with different cable resistance (\( R_{\text{cable}} = 0.8 \Omega \) and \( R_{\text{cable}} = 0.2 \Omega \)). Figure 6 shows the simulation results when the line is 110VAC(rms) and the common load current \( I_L \) experiences a sudden increase (1A→2A) at \( t=80\text{ms} \). Figure 7 also shows the simulation results but with a 220VAC(rms) line and the common load current experiences a sudden increase (2A→4A) at \( t=80\text{ms} \). Tables I and II give the input current harmonic levels of each module. It can be noticed from Figs. 6 and 7 that the system is stable and good current sharing has been achieved.

![Fig. 5. Voltage loop gain for each ac-dc converter.](image)

| Table I. Harmonic contents of each PFC converter with 110VAC line and 1A common load current |
|---|---|---|---|---|---|---|
| Current (mA, rms) | \( I_1 \) | \( I_3 \) | \( I_5 \) | \( I \) | THD | pf |
| \#1 (\( R_{\text{cable}} = 0.8 \Omega \)) | 226 | 20.3 | 0.88 | 226.9 | 8.9% | 0.996 |
| \#2 (\( R_{\text{cable}} = 0.2 \Omega \)) | 226.7 | 20.8 | 0.86 | 227.7 | 9.2% | 0.996 |

| Table II. Harmonic contents of each PFC converter with 220VAC line and 2A common load current |
|---|---|---|---|---|---|---|
| Current (mA, rms) | \( I_1 \) | \( I_3 \) | \( I_5 \) | \( I \) | THD | pf |
| \#1 (\( R_{\text{cable}} = 0.8 \Omega \)) | 235.9 | 43.5 | 6.1 | 240 | 18.6% | 0.983 |
| \#2 (\( R_{\text{cable}} = 0.2 \Omega \)) | 234.8 | 44.1 | 6.2 | 239 | 19% | 0.982 |

Loop gain bandwidth of a system is closely related to the system transient response and it is a general guideline to design a large bandwidth control loop in dc-dc power supplies. Observations from Figs. 6 and 7 show that rise time is shorter with high line (220VAC) than it is with low line (110VAC). This result coincides with the bode plot in Fig. 7 where one can easily recognize that the crossover frequency is much lower than 16.7Hz when input line is low. Referring to tables I and II, however, it is noticed that input current distortion is much smaller with low line. This once again confirms that the bandwidth of voltage loop gain should be low for PFC converters and should be smaller than the line frequency, which is in sharp contrast to the design of dc-dc converters.

V-260
5. CONCLUSION

Closed loop compensator design for a distributed power system was described in this paper. The design took into account power quality issues when PFC converters are included in the DPS. Simulation results showed that through proper design, the DPS utilizing central limit control could achieve both high power factor on the input side and precise and stable current distribution on the output side even when the system undergoes large variations in its operation conditions (100% increase in \( I_0 \) under 110VAC and 220VAC input voltage).

6. REFERENCES

[6]. L. R. Lewis, etc., “Modeling, analysis and design of distributed power systems,” PESC’89, pp. 152-159.