A NEW SWITCHED-CAPACITOR DC-DC CONVERTER
WITH IMPROVED LINE AND LOAD REGULATIONS

Guangyong Zhu, Huai Wei, Issa Batarseh and Adrian Ioinovic

Dept. of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816
Email: batarseh@mail.ucf.edu

Electrical Engineering and Electronics Dept.
Center for Technological Education Holon
Holon 58102, Israel
adrian@barley.cteh.ac.il

ABSTRACT

A new switched-capacitor (SC) step-down dc-dc converter is presented. It exhibits smaller size, lighter weight and stronger regulation capabilities than previous SC converters of the same power ratings. Its operation principles and analysis are described in detail and an accurate as well as an approximate expression governing input, output and circuit parameters is presented. A discussion on the achievable conversion efficiency is also given. A 12V/5V prototype based on the proposed topology has been implemented and tested. Theoretical prediction of its regulation and efficiency is verified experimentally.

1. INTRODUCTION

The rapid development of the modern electronic technology and equipment in computer and communications puts forward more critical requirements for efficient, small and light power supplies. A number of soft-switching techniques have been developed which have pushed the switching frequency in switched-mode power supplies of several tens kilohertz twenty years ago to the present stage of higher than 500kHz, resulting in more efficient and compact power supplies. Further increasing the switching frequency helps but can not solve completely the problem, due to the fact that the existing converters contain bulky magnetic elements such as transformers and inductors. These magnetic elements are essential components for the controlled transfer of energy. They are also responsible for the extra stresses on switches and other components in the power supplies.

It is therefore a new research area in power electronics emerged which renounces the use of any magnetic element and solely relies on switches and capacitors to accomplish the energy transfer task previously accomplished by inductors and/or capacitors in many switched-mode power converters. By controlling the time duration of charging and discharging of the capacitors, the switches and capacitors can form a switched-capacitor network that switches among different predetermined topological stages and provides a stable output to the load. Because of no magnetic devices, the SC circuit features small size, light weight, gives less EMI problems and makes it possible for the whole converter to be manufactured on a single IC chip.

Unlike in traditional switched-mode power converters where controlled power transfer are easily achieved because of the presence of input inductors, power transfer in SC converters is hard to be controlled and is normally accompanied by a comparable amount of power loss [4,5]. This makes it difficult for SC converters to obtain efficient energy conversion. It is known that when charging a capacitor from a voltage source, power loss may occur regardless of the parasitics (on-resistance of switches and ESR-equivalent series resistance of capacitors) and this loss is only dependent on the capacitor value and the difference between the input source and the initial as well as the final capacitor voltages. On the other hand, these parasitics play an important part in the choice of switching frequency. They are also one of the main factors that affect the resulting regulation capability.

A number of papers have contributed to the analysis of SC converters [1,4,5]. It was demonstrated in [1] that the maximum conversion ratio for a given number of capacitors k follows the elegant A-th Fibonacci series, and that the bound on the number of switches required satisfies 3k-2. However, the regulation capability of those converter topologies was not studied. While state-space averaging method was used extensively in deriving the input-output conversion ratios in SC circuits [2-3], some important design parameters such as capacitor values, switching frequencies were lost and optimum design with respect to high efficiency and good regulation could not be achieved. An accurate analysis of SC converters can be found in [4] where the dependence of converter performance upon circuit parameters and configurations was established and design guidelines were provided.

SC converters are very attractive in low power applications. Some successful designs and applications can easily be found in the literature [6]. However, previous SC converters suffered from either poor overall performance (large output ripple, poor efficiency or regulation) or increased complexity in circuit topology. In this paper, a new step-down SC converter will be studied which has a very simple topology. Yet it can provide very good line and load regulation. The proposed SC converter and its operation principle will be described in Section II. Its analysis, experimental results and conclusions are presented in the subsequent sections.

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2. OPERATION PRINCIPLE OF THE PROPOSED SC CONVERTER

The power stage of the new SC converter is shown in Fig. 1(a). The circuit is composed of two symmetrical parts: switches $S_1$-$S_4$, capacitor $C_1$, $D_1$, $D_4$ and $C_2$, $D_3$, $D_4$. The switches are turned on and off according to the timing diagram given in Fig. 1(b). Consequently the circuit goes through four topological stages in each switching cycle.

![Diagram of the SC converter](image)

Fig. 1. (a) Step-down SC converter power stage; (b) Timing diagram for switch operation.

The periodical operation of the converter can be understood as follows: in the first stage, capacitor $C_1$ as well as the output capacitor $C_0$ is charged in series by the input source for a limited time $dT_1$, where $d$ is the duty cycle ($0<d<0.5$) and is determined by the feedback control circuit. At the same time, $S_4$ is turned on and capacitor $C_2$ is connected to the load in parallel with $C_0$, enabling the energy accumulated in $C_2$ during the second half cycle of the previous switching period to transfer to the load. In the second stage, only $S_4$ is on and capacitor $C_2$ is continuously discharged to the load until $t=T/2$ when $S_4$ is turned off and $S_2$, $S_3$ are turned on. In the second half-cycle (stage 3 and 4), $C_2$ is charged in series with $C_0$ by the input source for a period of $dT_2$ and the energy accumulated in $C_1$ during the first half cycle is transferred to the load. The role of $C_1$ and $C_2$ interchanges when the next switching cycle begins.

It should be pointed out that the inclusion of the output capacitor $C_0$ in the charging process and the symmetrical circuit operation of $C_1$ and $C_2$ bring a number of salient features to the converter as compared with previous SC circuits, such as the ones presented in [2] and [3]. First, inclusion of $C_0$ helps to reduce two capacitors and two diodes for the same voltage conversion ratio in [2]. This not only reduces the converter size and weight, as we will see later, it also increases converter's ability to provide a stable output voltage with a smaller input; thus improves regulation capability. Second, symmetrical circuit operation increases the equivalent output filtering capacitance ($C_{dp}+C_{dp}$ or $C_{dp}+C_{dp}$). Therefore the output voltage ripple is expected to be smaller than those in [3] where only $C_0$ was present to hold the output voltage when charging process was over.

Another advantage of the proposed SC circuit is its expandability to provide different step-down conversion ratios such as 12V/5V, 12V/3.3V without degrading conversion efficiency. This can be done by adding more capacitors and diodes in the charging/discharging branches.

3. ANALYSIS OF THE SC CONVERTER

To find the DC voltage conversion ratio, the well-known state-space averaging technique is applied. For each of the four switching stage, state equation in the form $\dot{x} = A_x x + B_x u, \ k=1, 2, 3$ and 4 and can be derived, where $u=[v_{in}, V_d]^T$, $x=[v_{C1}, v_{C2}, v_o]^T$, and $V_d$ denotes the forward voltage drop of the conducting diode. From formula $X = -A_{xav} B_{xav} U$, where $A_{xav}$ and $B_{xav}$ are averaged state matrices, it turns out that

$$V_o = \frac{V_i - 2V_d}{2 + \frac{1}{R} \left( \frac{r_1 + r_2 + r_p + r_q}{4d} \right)},$$

(1)

where $r_p$ denotes the ESR of each capacitor, $r_1$ and $r_2$ the on-resistance of switches $S_1$, $S_2$ and $S_3$, $S_4$, respectively. From Eq. (1) it can be seen that if there is any variation in the input voltage or the load, $d$ can be adjusted accordingly to keep a stable output voltage.

To see the regulation capability of the converter, $d$ is plotted against $V_{in}$ for a constant load (Fig. 2(a), 5V@3.5A) and against $I_o$ for a constant line (Fig. 2(b), 12V) with the following parameters: $r_p=0.02\Omega$, $r_1=0.3\Omega$ (IRF9530), $r_2=0.085\Omega$ (IRF540), and $V_d=0.3V$ (1N5823). It can be noticed that the proposed SC converter can sustain an output of 5V@3.5A even when the line varies from 11.4V to 16V, or it can provide a wide range of load current from 0.2A to 6.5A with a 12V input voltage. This result indicates a much better regulation capability for the proposed converter as compared with the one presented in [2] for the same 12V/5V conversion, where only a maximum 3A load and a minimum 11.8V input could be realized under nominal operation conditions.

Although the above results are obtained from the approximate state-space averaging approach, for many
practical applications, Eq. (1) can provide a good insight in understanding the input/output relationship of the converter. More accurate expression for the converter can be obtained by applying the technique described in [4] and it gives:

\[
\eta = \frac{2V_o}{V_m}
\]

(3)

Equation (3) may be skeptical at the first glance as it shows that the conversion efficiency of the SC converter merely depends on the input and output voltage levels. It claims that the proposed SC converter will have 83.3% efficiency (2×5/12) for the 12V/5V operation. And it does not depend on circuit parasitics and load current. As a matter of fact, these factors affect the efficiency indirectly, as can be explained with Eq. (2). Any variations in circuit parameters and load current will invoke a corresponding change in \( d \) such that the output is to be kept constant. If these variations tend to cause \( d \) to move out of its operation limit (0.5 in this circuit), a voltage drop in the output can be expected or a higher input voltage must be applied, resulting in a decrease in the conversion efficiency. This interesting phenomenon is in fact a common characteristic for SC converters powered from voltage sources. For example, if this circuit is expanded to perform a 12V/3.3V conversion, the resulting efficiency will be 82.5% (3V/3V) under nominal operation conditions.

4. EXPERIMENTAL VERIFICATION

A 12V/5V prototype as proposed in Fig. 1 has been implemented and tested by using multi-layer ceramic capacitors (they are characterized by small ESRs) of 47μF for \( C_1, C_2 \) and of 100μF for the output capacitor \( C_o \). A simple PWM IC chip (SG3525) was used to generate the required switching signals. A number of practical issues are essential to the successful design and implementation of this converter. First, one may notice from Eq. (1) that it seems the smaller the parasitic resistance (capacitor ESRs and switch on-resistances), the smaller the load resistance \( R \) for the same variation of the duty cycle \( d \), which means a larger output power can be obtained. However, smaller parasitic resistance increases the inrush current and may damage the converter at its start-up. Second, to avoid simultaneous conduction of switches \( S_1 \) and \( S_2 \) (or \( S_3 \) and \( S_4 \)) at the beginning of each half-cycle (Fig. 1(b)), the turn-on signal to \( S_1 \) (or \( S_2 \)) was delayed about 0.1μs after \( S_1 \) (or \( S_4 \)) had been turned off. This will prevent the input source from being applied to the load via the conducting switches. Third, to simplify the feedback control circuit design, P-channel power MOSFETs were chosen for switches \( S_1 \) and \( S_2 \). As their source terminals were connected to the 12V input source, they can be safely turned on with a logic "0" signal. P-channel MOSFETs also help to limit the inrush current because of their large on-resistances over some of their N-channel counterparts.

Analysis of Eq. (2) shows that if low switching frequency operation is designed such that condition \( dT_s << \tau \) is violated, regulation capability of the resulting converter would be inversely affected. On the other hand, experimental result showed that at high switching frequencies, the effect of parasitic inductance in the capacitors became nonnegligible, causing resonance in the voltage and current waveforms, particularly at the switching instants. As a result, the switching frequency was chosen to be 165kHz to compromise the design trade-off.

Figure 2 compares the theoretical and experimental duty cycles with variations in line or load under nominal
load or nominal line. It is believed that the small discrepancies are mainly a result of variations in parasitic resistance at dc and at high switching frequency.

Steady-state voltages across the capacitors have been recorded in Fig. 3 under a 5V@3.5A output. Except for some transient peaks, the capacitor voltages are very stable.

![Image of voltage waveforms across capacitors]

**Fig. 3. Steady-state voltage waveforms across capacitors.**

It was observed from the measurement that the input current did not change as long as the load was kept constant and the line voltage was within its regulation range, and this input current varied proportionally with the load current as long as the line voltage was kept constant. These phenomena clearly verify that the conversion efficiency of the SC converter is solely determined by the conversion ratio as predicted by Eq. (3). Fig. 4 shows the measured conversion efficiency under nominal input voltage.

![Image of conversion efficiency graph]

**Fig. 4. Conversion efficiency of the SC-converter.**

Line and load regulation capability of the proposed SC-converter is shown in Fig. 5. At larger load, the lower and upper band of the line voltage increases since larger input voltage is required to compensate for the increased voltage drops on the circuit parasitics. From Fig. 5, it can be seen that the converter can provide a 0.5A to 6.2A output current with the nominal 12V input or can provide a stable 3.5A current even when the input changes between 11.43V and 16.5V. Because of the inefficient operation under high line input (efficiency becomes lower than 60% when input voltage is higher than 16.5V), measurement of line regulation was not conducted for input voltage beyond this range.

![Image of regulation capability graph]

**Fig. 5. Regulation capability of the SC-converter.**

5. CONCLUSION

A new SC dc-dc converter topology is presented. It has fewer components than step-down SC converters reported in the literature, yet it accommodates a much wider range of line and load variations. Experimental results showed that the proposed SC converter can operate with an input voltage as low as 10.45V at light load and can provide an output current of more than 6A at 12V input. A conversion efficiency of over 80% can be achieved under nominal 12V/5V operation. Because of the easy expandability of the proposed converter structure, it is suitable for applications where low power rating, low voltage power supplies are required.

6. REFERENCES


