

A Modified Control Scheme to Alleviate DC Voltage Stress in Active Clamp PFC AC/DC Converter with Universal Input¹

Wenkai Wu[†], Weihong Qiu, Wei Gu and Issa Batarseh

[†]APECOR Co.

Research Pavilion #453

12424 Research Park, Orlando, FL 32826

School of Electrical Engineering and Computer Science

University of Central Florida

Orlando, FL 32816

Tel. (407) 823-0185 Fax (407) 823-6334

Email: batarseh@mail.ucf.edu

Abstract: A modified control scheme is proposed to alleviate bulk capacitor voltage stress in active clamp Bi-flyback Power Factor Correction (PFC) AC/DC converter with universal input. In the proposed control scheme, the auxiliary switch is turned on with a fixed narrow pulse-width, rather than the conventional complimentary signal of the main switch. As a result, the proposed technique will substantially suppress the DC voltage well below 400V under the entire input range. The improved performance was experimentally verified through a 28V@5.35A prototype.

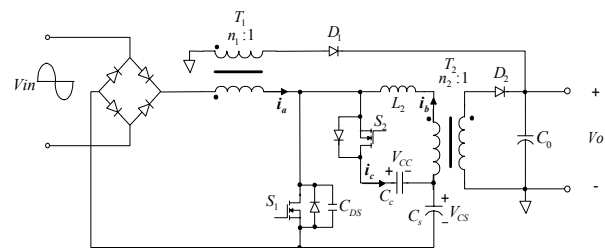
I. INTRODUCTION

Active Power Factor Correction (PFC) technique continues to be attractive research topic with several effective regulations being reported. Conventional cascade of two-stage topology can achieve good performance such as high power factor and low voltage stress, but it usually suffers from high cost and increased circuit complexity. Many single-stage PFC AC/DC converters have been proposed that can be applied cost-effectively [1,2]. However, it's well known that in single stage topologies, the voltage across the bulk capacitor can not be controlled well due to the fact that only one switch and control loop are used. Moreover, the storage capacitor voltage varies widely with the input voltage and load variation, especially when the PFC cell operates in DCM mode while DC/DC stage operates in CCM mode. Finally, the storage capacitor voltage will increase to be unbearable under light load condition.

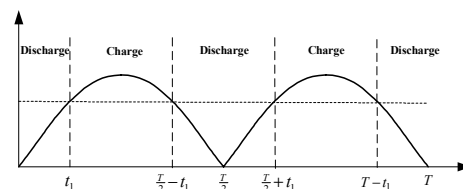
Recently, several approaches were proposed to suppress the DC voltage stress. In reference [3], Chow introduced frequency modulation method to alleviate the voltage stress, while the varied frequency brought about the EMI issues and increases magnetic component design difficulty. Another approach is to keep the DC/DC stage operating in DCM mode under full load range [4], while DC/DC stage prefers CCM mode due to low output ripple and higher efficiency. Proposed method in [5,6] aimed at achieving a compromise between THD and voltage stress by introducing negative voltage feedback with an additional transformer winding

serially connected with the boost inductor. However, the dead angle in input current when input voltage below the feedback voltage increases the THD and limits its application.

It's shown that the newly proposed Bi-flyback AC/DC topologies in [7,8] can effectively alleviate the DC bus voltage, while a drawback to the use of the flyback is the relatively high voltage and current stress suffered by its switching components. Switch voltage stress could be minimized by incorporating an active clamp circuit that serves to limit the turn-off voltage spike while recycling the flyback transformer leakage energy [9,10]. Therefore, an active clamp Bi-flyback topology, as shown as Fig. 1(a), is adopted in this paper as a PFC AC/DC converter with universal input. There are actually two flyback transformers, PFC flyback transformer T_1 and DC/DC flyback transformer T_2 , their operation principles will be detailed in Section II. C_s is the bulk capacitor to provide DC voltage bus, which is charged around high line voltage area, and discharged during low line voltage period in one line cycle, as shown as Fig. 1 (b), to obtain low output voltage ripple.



(a) Topology



(b) Operation modes of C_s in one line cycle

Fig. 1: Active clamp Bi-flyback converter

¹ This work was partially supported by NASA-STTR phase II grant # NAS10-00038

For active clamp Flyback topology introduced in [9,10], the auxiliary switch is usually turned on and off alternatively with the main switch, achieving soft switching condition simultaneously for both switches. However, in such control mode, the DC bus voltage still stay beyond the tolerance of commercially available capacitor. In this paper, a modified control scheme aiming at further alleviating the DC bus voltage to below 400V through the universal input range, without sacrificing the efficiency and the power factor, is proposed and experimentally verified.

II. PROPOSED CONTROL SCHEME AND THE PRINCIPLE OF OPERATION

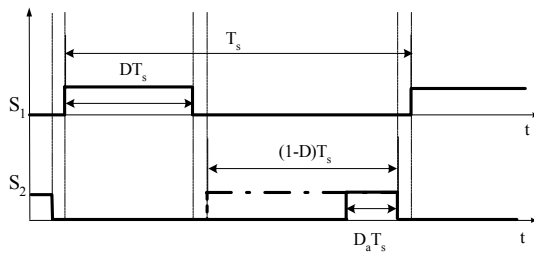


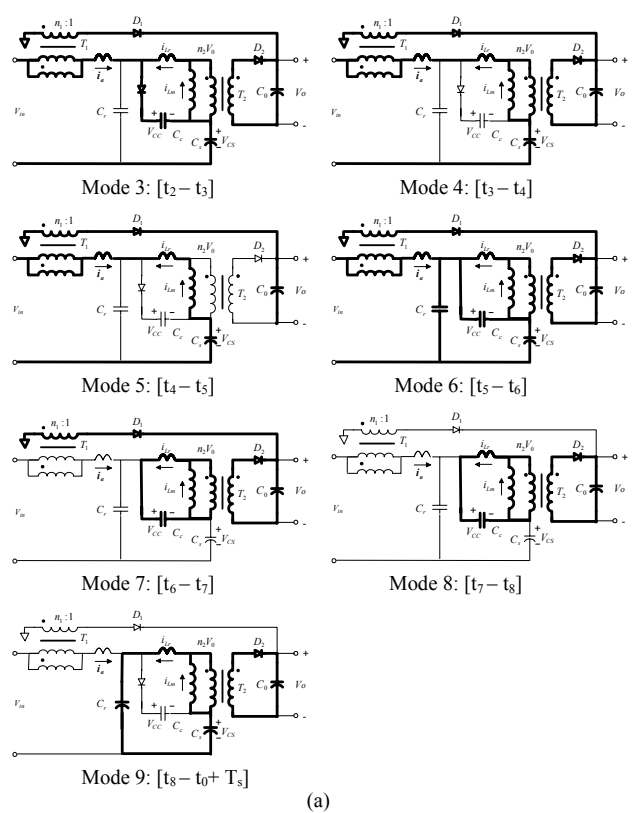
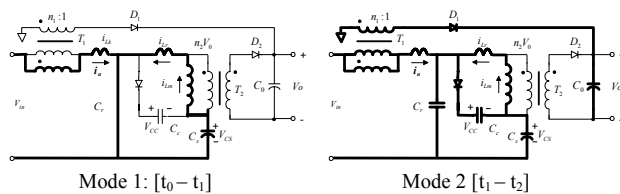
Fig. 2 Modified control scheme

The control scheme for the proposed converter is shown as Fig. 2. The auxiliary switch is turned on with a fixed narrow pulse width $D_a T_s$, rather than the conventional complimentary signal of the main switch ($(1-D)T_s$) in the active clamp application [9].

In the Bi-flyback AC/DC converter presented in [7], the operation mode of transformer T_1 and T_2 varies in one line cycle, depending on the charge or discharge condition of bulk capacitor, which is governed by the equation: $V_{in}(t) + n_1 V_0 = V_{cs} + n_2 V_0$. Therefore, here we can also divide one line cycle into charge and discharge intervals to analyze the operation principle of active clamp Bi-flyback converter, afterwards to illustrate how the modified control scheme works.

The following discussion takes into account the leakage inductance of both transformers, and assume that:

- All components are ideal;
- Leakage inductance much less than the magnetizing inductance for both flyback transformers: $L_k \ll L_b$ for T_1 and $L_r \ll L_m$ for T_2 .



(a)

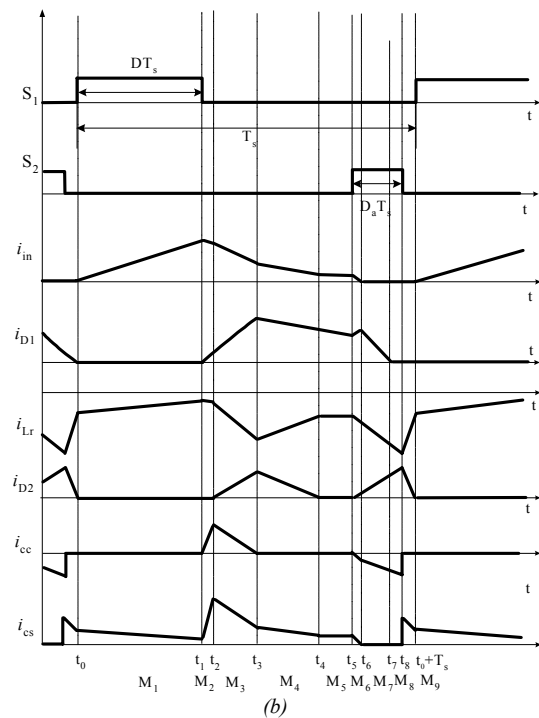


Fig. 3 (a) Operation modes, and (b) key waveforms in charge interval

A: Charge Interval

The operation modes and key waveforms in charge interval are illustrated in Figs. 3(a) and (b) respectively. The detailed operation of the circuit can be explained as follows with focusing on the current variation flowing through the bulk capacitor.

Mode 1: $[t_0 - t_1]$

At t_0 , S_1 is turned on while S_2 is off, as shown in Fig. 3 (a). The output rectifiers D_1 and D_2 are reverse biased. For T_1 , the magnetizing inductance L_b , together with the leakage inductance L_k , is charged linearly up according to the Equations:

$$(L_B + L_k) \frac{di_{in}}{dt} = V_{in}$$

For T_2 , the magnetizing inductance L_m , together with the resonant inductance L_r , is also charged up linearly. And the current flowing through bulk capacitor i_{cs} decreases linearly according to the Equation:

$$(L_r + L_m) \frac{di_{cs}}{dt} = V_{cs}$$

Mode 2: $[t_1 - t_2]$

At t_1 , S_1 is soft turned off due to the existence of switch parasite capacitance C_r . Since the charging duration is relatively short, this soft turning off duration could be neglected here to simplify the analysis.

When V_{Cr} increases to the value of V_{Cs} , i_{in} will be diverted to charge C_c and C_s . Since $C_c \gg C_r$, current can be considered totally flowing through C_c .

Since the secondary voltage of transformer T_1 is sufficient to forward bias D_1 , the primary voltage of T_1 is then clamped to approximately n_1V_0 . Therefore, in this period we have the following governing equations:

$$L_k \frac{di_{cs}}{dt} = V_{in} + n_1V_0 - (V_{cs} + v_{cc})$$

$$i_{cs} = -i_{Lr} + C_c \frac{dv_{cc}}{dt}$$

$$(L_r + L_m) \frac{di_{Lr}}{dt} = v_{cc}$$

Due to $L_m \gg L_r$, i_{Lr} can be considered to be constant $i_{Lr} \approx I_{Lr}$ to simplify the analysis, so:

$$i_{cs} = \sqrt{\frac{\Delta^2}{L_k} + I_{Lr}^2} \sin\left(\frac{t}{\sqrt{L_k C_c}} + \tan^{-1} \frac{I_{Lr}}{\Delta} \sqrt{\frac{L_k}{C_c}}\right) \quad (1)$$

where, $\Delta = V_{in} - n_1V_0 - V_{cs}$.

Mode 3: $[t_2 - t_3]$

At t_2 , when voltage across clamp capacitor V_{Cc} increases until $V_{cc} \cdot \frac{L_m}{L_r + L_m} \geq n_2V_0$, D_2 becomes also forward biased and T_2 operates in forward mode. The transformer primary voltage is clamped, by the large output capacitance, to approximately n_2V_0 . Equations of this mode are:

$$(L_r + L_k) \frac{di_{Lr}}{dt} = -(V_{in} + n_1V_0) + (V_{cs} + n_2V_0)$$

$$L_r \frac{di_{Lr}}{dt} = -v_{cc} + n_2V_0$$

$$i_{cs} = -i_{Lr} + C_c \frac{dv_{cc}}{dt}$$

Since V_{Cs} can be considered constant, so current flowing through bulk capacitor i_{cs} decrease near linearly.

Mode 4: $[t_3 - t_4]$

At $t = t_3$, current flowing through C_c reaches zero with $i_{cs} = i_{Lr} = i_{in}$, V_{Cc} then reaches its maximum value, blocking the body diode of auxiliary switch S_1 . The current i_{cs} decreased according to the following Equation:

$$(L_r + L_k) \frac{di_{cs}}{dt} = -(V_{in} + n_1V_0) + V_{cs} + n_2V_0$$

Mode 5: $[t_4 - t_5]$

At $t = t_4$, D_2 is reverse biased and i_{cs} decreased linearly by the following relationship:

$$(L_r + L_m + L_k) \frac{di_{cs}}{dt} = -(V_{in} + n_1V_0) + V_{cs}$$

Since $L_m \gg L_r$, i_{cs} almost kept constant.

Mode 6: $[t_5 - t_6]$

At $t = t_5$, turn on S_2 , V_{Cc} applied upon transformer T_2 with its primary voltage again clamped to n_2V_0 . By neglecting the effect of C_r , we have:

$$L_r \frac{di_{Lr}}{dt} = V_{cc} - n_2V_0$$

$$L_k \frac{di_{cs}}{dt} = (v_{cc} + V_{cs}) - (V_{in} + n_1V_0)$$

$$i_{cs} = -i_{Lr} + C_c \frac{dv_{cc}}{dt}$$

Mode 7: $[t_6 - t_7]$

At $t = t_6$, $i_{in} = i_{cs} = 0$, and we have

$$v_{cc} - n_2V_0 = L_r \frac{di_{Lr}}{dt}$$

$$i_{Lr} = -C_c \frac{dv_{cc}}{dt}$$

Since we assume $C_c \gg L_r$, i_{Lr} increases linearly as shown in Fig.3 (b).

Mode 8: $[t_7 - t_8]$

The operation mode is almost the same as Mode 7, except there is no current flowing through the secondary of transformer T_1 .

Mode 9: $[t_8 - t_0 + T_s]$

The auxiliary switch is turned off at t_8 , effectively removing C_c from the circuit. At this moment, the magnetizing current diverted to the bulk capacitor is given by:

$$i_{cs}(t)|_{t=t_8} = i_{Lr}(t)|_{t=t_8} = \frac{V_{cc} - n_2V_0}{L_r} D_a T_s \quad (2)$$

In this mode, a resonant network is formed between L_r and main switch drain to source capacitance C_r . The primary voltage of the transformer T_2 remains clamped at n_2V_0 as C_r is discharged to provide soft switching condition for the main switch. The first order differential equation in terms of C_r and L_r are given by:

$$L_r \frac{di_{Lr}}{dt} = V_{cs} + n_2V_0 - v_{cr}$$

$$C_r \frac{dv_{cr}}{dt} = i_{Lr}$$

At $t = t_0 + T_s$, D_2 is reverse biased by V_0 . The magnetizing and leakage inductances of both transformers begin to linearly charge again, starting another switching cycle.

B: Discharge Interval

The operation modes and key waveforms in discharge interval are illustrated in Figs. 4(a) and (b) respectively. The brief description of operation can be explained as follows:

Mode 1: $[t_0 - t_1]$

Same as Mode 1 in the charging interval in Fig. 3(b).

Mode 2: $[t_1 - t_2]$

Same as Mode 2 in the charging interval in Fig. 3(b).

Mode 3: $[t_2 - t_3]$

At t_2 , when voltage across clamp capacitor V_{cc} becomes $V_{cc} \frac{L_m}{L_r + L_m} \geq n_2V_0$, D_2 is forward biased and T_2 operates in flyback mode. The transformer primary voltage is clamped by the large output capacitance to approximately n_2V_0 . The equation in this mode are given by:

$$C_c \frac{dv_{cc}}{dt} = i_{cc}, \quad C_r \frac{dv_{cr}}{dt} = i_{cc} + i_{Lr}$$

$$v_{cr} = v_{cc} + V_{cs}, \quad L_r \frac{di_{Lr}}{dt} = v_{cc} - n_2V_0$$

$$i_{cs} = i_{cc} - i_{Lr}$$

Since it is assumed that $C_c \gg C_r$, current can be considered flow fully through C_c .

Mode 4: $[t_3 - t_4]$

In this mode, current i_{cs} reaches zero, and we have:

$$L_r \frac{di_{Lr}}{dt} = v_{cc} - n_2V_0$$

$$C_c \frac{dv_{cc}}{dt} = i_{Lr}, \quad i_{Lr} = i_{cc}$$

Mode 5: $[t_4 - t_5]$

Same as Mode 4 except there is no current flowing through the secondary of transformer T_1

Mode 6: $[t_5 - t_6]$

At $t = t_5$, i_{Lr} reach zero and clamp capacitor C_c is blocked by the reverse biased body diode of S_2 , L_r will resonant with C_r according to the following equation:

$$L_r \frac{di_{Lr}}{dt} = V_{cs} + n_2V_0 - V_{cr}$$

$$C_r \frac{dV_{cr}}{dt} = i_{Lr}$$

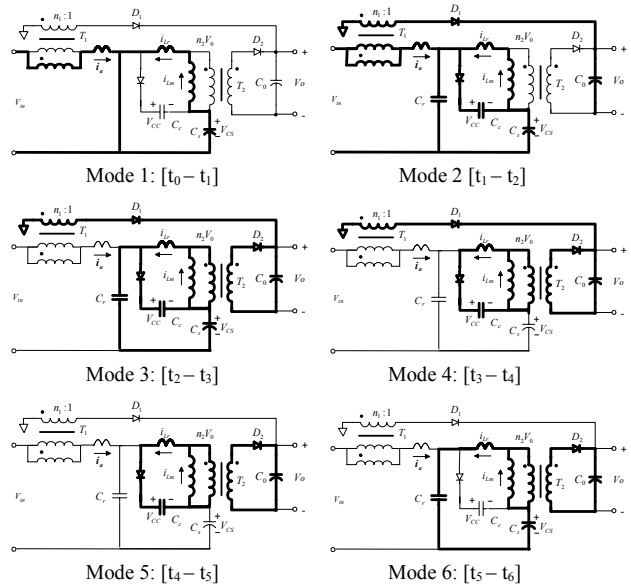
Mode 7: $[t_6 - t_7]$

Same as Mode 8 in the charging interval in Fig. 3(b).

Mode 8: $[t_7 - t_0 + T_s]$

Same as Mode 9 in the charging interval in Fig. 3(b).

At $t = t_0 + T_s$, D_2 becomes reverse biased by V_0 . The magnetizing and leakage inductances of both transformers begin to linearly charge again, starting another switching cycle.



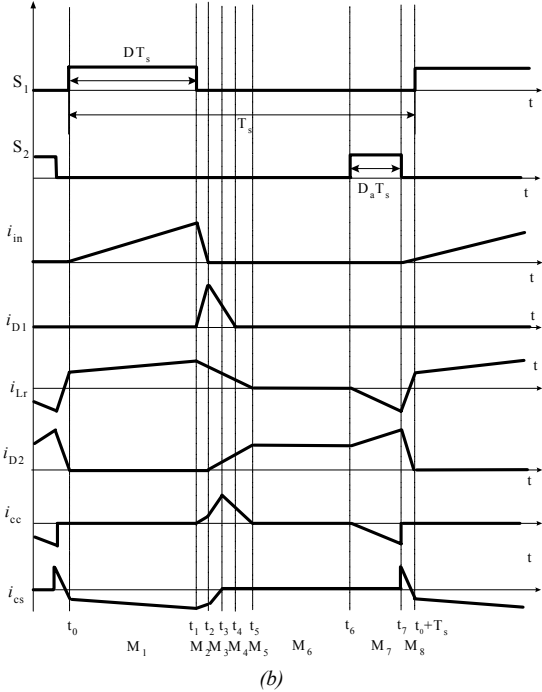
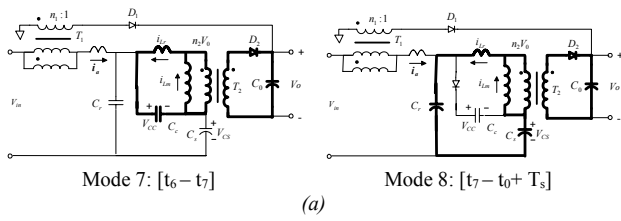


Fig. 4 (a) Operation modes, and (b) key waveforms in discharge interval

From the afore-description, the operation condition of the bulk capacitor in each switching cycle could be determined through the current variation flowing through it.

From bulk capacitor current waveform i_{cs} in Fig. 3 and Fig. 4, it can be easily concluded that the ON time of auxiliary switch did affect the bulk capacitor voltage stress. We note:

- 1) For both charge and discharge intervals, at the instant of turning off the auxiliary switch, the discharging current of clamp capacitor diverted to the bulk capacitor, since this current is proportional to the ON time of auxiliary switch, as shown by Equation (2). Therefore, reducing the length of ON time can effectively alleviate the voltage stress across the bulk capacitor.
- 2) Due to cost and size considerations, the clamp capacitor is pretty small compared to the bulk capacitor, therefore, larger ON time will lead to lower final voltage across the clamp capacitor at the moment of the auxiliary switch being turned off. Since D_2 is forward biased until V_{cc} increases to the value

$$V_{cc} \frac{L_m}{L_r + L_m} \geq n_2 V_0, \text{ it's easy to conclude from Equation}$$

(1), that just after turning on the main switch, the lower V_{cc} will result in more current charged to the bulk capacitor in the next switching cycle. If V_{cc} was kept higher value, partial current could have been transferred to the output through the secondary winding of PFC Flyback transformer.

III. FEATURES OF PROPOSED CONTROL SCHEME

From afore-description, the features of the proposed control scheme can be summarized as follows:

1. Higher efficiency can still be achieved due to soft switching operation of the main switch.
2. With the proposed control scheme, the DC bus voltage stress can be alleviated remarkably; this is attractive feature to universal input applications. Low DC bus voltage makes it possible to use only one commercial off the shelf (COTS) storage capacitor. Moreover, low voltage rated components can be used in the power stage, which can further reduce the cost and improve the efficiency. Since $R_{dson} \approx kV^2_{bvdss}$ for MOSFET and $V_{fw} \approx kV^2_{rrm}$ for rectifiers.
3. Even though the auxiliary switch sacrificed its soft-switching turned on condition, its narrow ON time allow us to choose low current rated MOSFET. Hence the switching loss of the auxiliary switch is pretty small due to reduced parasite capacitance.
4. Direct energy transfer from transformer T1 helps to increase the overall efficiency due to partial power transferred to the output just being processed once. Also, the soft switching makes the high frequency operation possible; therefore, the power density can be increased.

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the above analysis, a 28V@5.35A PSPICE closed loop simulation circuit is built up as shown as Fig. 5.

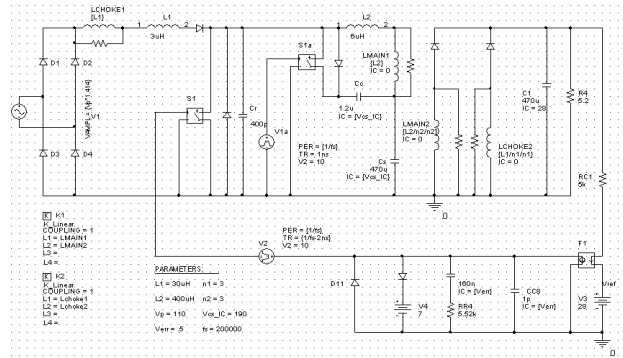
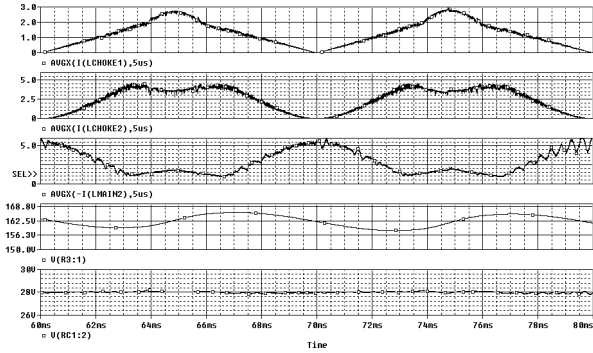
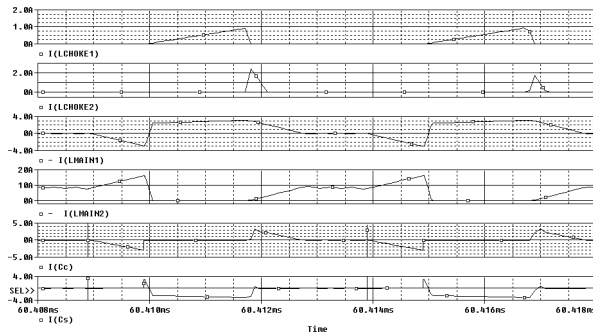


Fig. 5 Simulation Schematics

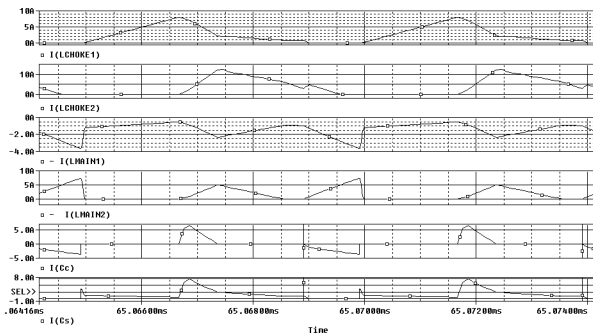


(a) Waveforms in one line cycle

(First trace: Rectified input current;
 Second trace: Current transferred to the output through T2;
 Third trace: Current transferred to the output through T1;
 Fourth trace: Voltage across bulk capacitor;
 Fifth trace: Output Voltage)



(b) Current flowing through different components in charge interval



(c) Current flowing through different components in discharge interval

Fig. 6 Simulation results

Figure 6 gives the simulated results for the proposed control for a specific design example. Fig. 6(a) presents key waveforms in one line cycle: The first trace shows the rectified input current, which is nearly sinusoidal waveform with unity power factor; The second trace indicates the current transferred to the output through T1, resulting in more than 50% energy transferred to the output side without processed twice, as previous approach did. This helps to increase the overall efficiency of the converter; The third

trace indicates current transferred to the output through T2, which just fills the valley of the second current trace to pursue the trade-off between the high power factor and low output ripple; Fourth trace shows the charge and discharge variations of the bulk capacitor, which also clearly indicates the transition of transferring power through T1 or T2; The last trace gives the output voltage to indicate the active clamp Bi-flyback topology with the modified control scheme can obtain pretty small output ripple with near unity power factor.

Figures 6(b) and (c) show the current flowing through the different components in one switching cycle during charge and discharge intervals respectively, which agreed well with the discussion in Section II.

A 85~265V/60Hz input, 28V@5.35A output prototype was built to experimentally verify the modified control scheme. The following key components were used in the implementation of the experimental circuit: Input transformer T1: $N_p1:N_s1= 21:7$, $L_{k1}=3\mu\text{H}$; DC/DC transformer T2: $N_p2:N_s2= 30:10$, $L_{k2}=6\mu\text{H}$; Switches— S1: IXFH20N60; S2: IRFPC30C; Storage Capacitor — 470 $\mu\text{F}/450\text{V}$; Clamp capacitor — 1.2 $\mu\text{F}/200\text{V}$; Boost Diode — DSEI 1210A; Secondary rectifier diode D1, D2 — MUR3020; Switching frequency — 200kHz.

Figure 7 gives the measured maximum voltage across C_s with the different ON time of the auxiliary switch. It can be seen that the smaller the ON time, the lower the voltage. Therefore, the criterion for determining the ON time is as narrow as possible, providing the duration is wide enough to provide soft switching condition for the main switch. In the developed prototype, T_a is fixed at 450ns.

In Fig. 8, the maximum voltage across bulk capacitor in different input voltage is shown. As shown, the maximum voltage, occurred under 265V/AC input, is well below 400V.

Figures 9 and 10 present the full load efficiency and power factor through the entire input voltage range. The results indicate the efficiency and PF stay above 81% and 0.95 respectively, through the whole input range even operating under 200KHz.

Finally, Fig. 11 gives the measured line voltage and current waveforms, resulting in power factor of 0.987.

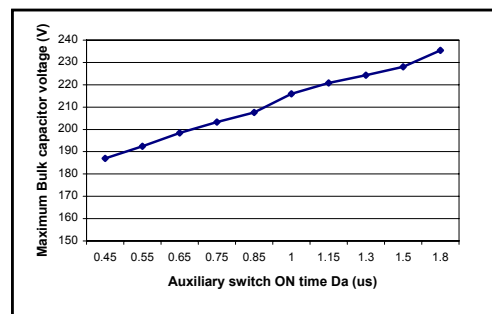


Fig. 7 Measured maximum bulk capacitor voltage in different auxiliary switch ON time ($V_{in}=110\text{Vac}$)

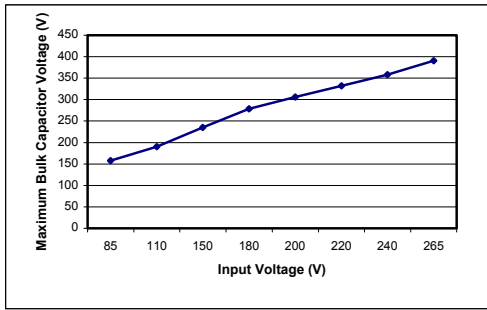


Fig.8 Measured maximum bulk capacitor voltage in different input voltage

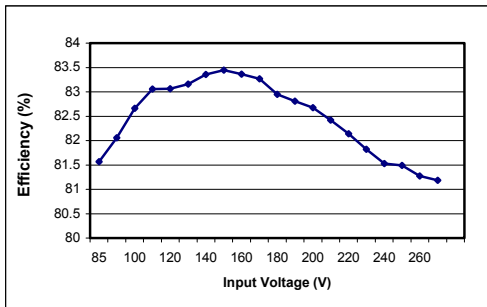


Fig. 9 Measured Efficiency vs. line voltage under full load

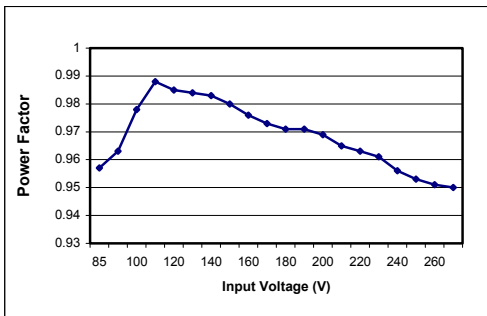


Fig.10 Measured power factor vs. line voltage under full load

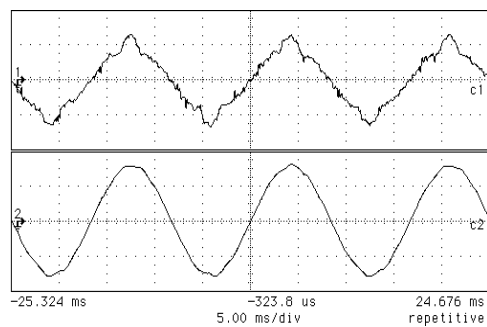


Fig. 11 Measured input current (upper trace 2A/div) and line voltage (lower trace 100V/div) under full load

V. CONCLUSION

In Bi-flyback active clamp PFC AC/DC converter, using a fixed narrow pulse width to control the auxiliary switch, rather than conventional complimentary signal of the main switch, is proposed. It is shown that the bulk capacitor voltage can be suppressed well below 400V through the entire input range, even when DC/DC stage operates in CCM mode. This feature permits the commercially available capacitors to be used for universal input application. The proposed control scheme achieves high power factor and still attain high efficiency due to the main switch operating in soft switching condition. The improved performance was experimentally verified through the construction of a 28V@5.35A prototype unit operating at 200kHz.

REFERENCES

1. Redl, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage," in Proc. PESC.94, pp. 1137-1144. June 1994.
2. F.-S. Tsai, P. Markowski, and E. Whitcomb, "Off-line flyback converter with input harmonic current correction," in Proc. INTELEC'96, 1996, pp. 120-124. 1996.
3. Chow, M.H.L.; Lee, Y.S.; Tse, C.K., "Single-stage single-switch isolated PFC regulator with unity power factor, fast transient response and low voltage stress," Proceedings of PESC98, pp.1422-1428, July 1998.
4. Rodriguez, E.; Canales, F.; Najera, P.; Arau, J., "A novel isolated high quality rectifier with fast dynamic output response," Proceedings of PESC97, pp. 550-555, July 1997.
5. Jinrong Qian; Qun Zhao; Lee, F.C., "Single-stage single-switch power-factor-correction AC/DC converters with DC-bus voltage feedback for universal line applications," Power Electronics, IEEE Transactions on, Volume: 13 Issue: 6, pp. 1079-1088, Nov. 1998.
6. Jindong Zhang; Lee, F.C.; Jovanovic, M.M., "An improved CCM single-stage PFC converter with a low-frequency auxiliary switch," Proceedings of APEC, pp. 77-83, March 1999.
7. Weihong Qiu, Wenkai Wu, Wei Gu and I. Batarseh, "A Bi-Flyback PFC Converter with Low Bulk Capacitor Voltage and Tight Output Voltage Regulation for Universal Input Applications," To be presented in APEC 2002.
8. Jin, C.; Ninomiya, T., "A novel soft-switched single-stage AC-DC converter with low line-current harmonics and low output-voltage ripple", PESC 2001, P660-665, vol.2, June 2001.
9. Robert Watson, Guichao Hua and Fred C. Lee, "Characterization of an Active Clamp Flyback Topology for Power Factor Correction Applications," Transactions on Power Electronics, Vol.11 No.1, pp. 191-198, Jan. 1996.
10. Watson, R.; Lee, F.C.; Hua, G.C. "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," Transactions on Power Electronics, Vol.11 No.1, pp. 162-169, Jan. 1996.